US009350360B2

(12) **United States Patent**
Sutardja

(10) **Patent No.: US 9,350,360 B2**
(45) **Date of Patent: May 24, 2016**

(54) **SYSTEMS AND METHODS FOR CONFIGURING A SEMICONDUCTOR DEVICE**

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(73) Assignee: **Marvell World Trade Ltd.**, St. Michael (BB)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Sep. 14, 2015**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 14/089,261, filed on Nov. 25, 2013, now Pat. No. 9,143,083, which is a continuation of application No. 11/486,557, filed on Jul. 14, 2006, now abandoned, which is a continuation

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(51) **Int. Cl.**
H03L 7/00 (2006.01)
H03L 1/02 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H03L 1/026*** (2013.01); ***G11C 5/00*** (2013.01); ***G11C 5/143*** (2013.01); ***H01L 23/10*** (2013.01); ***H01L 23/315*** (2013.01); ***H01L 23/345*** (2013.01); ***H03B 5/04*** (2013.01);

(Continued)

(58) **Field of Classification Search**
None
See application file for complete search history.

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Claim Recitation for U.S. Appl. No. 11/486,557, filed Aug. 4, 2009, 3 pages.

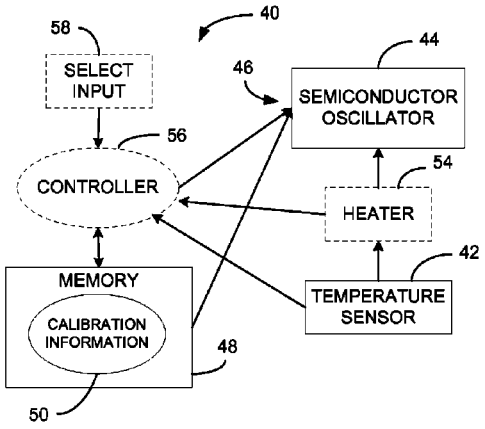
(Continued)

Primary Examiner — David E Graybill

(57) **ABSTRACT**

A system for configuring a semiconductor device to generate an output signal. The system includes a temperature sensor configured to sense a plurality of operating temperatures of the semiconductor device, the plurality of operating temperatures including at least a first operating temperature and a second operating temperature. A controller is configured to determine a plurality of operating frequencies of the output signal at respective operating temperatures of the plurality of operating temperatures. The plurality of operating frequencies include a first operating frequency of the output signal when the semiconductor device is at the first operating temperature and a second operating frequency of the output signal when the semiconductor device is at the second operating temperature. Memory is configured to store calibration information that associates each of the plurality of operating temperatures of the semiconductor device with respective operating frequencies of the plurality of operating frequencies.

20 Claims, 26 Drawing Sheets



Related U.S. Application Data

of application No. 11/328,979, filed on Jan. 10, 2006, now abandoned, which is a continuation-in-part of application No. 10/892,709, filed on Jul. 16, 2004, now Pat. No. 7,148,763, which is a continuation-in-part of application No. 10/272,247, filed on Oct. 15, 2002, now Pat. No. 7,042,301.

(60) Provisional application No. 60/756,828, filed on Jan. 6, 2006, provisional application No. 60/730,568, filed on Oct. 27, 2005, provisional application No. 60/714,454, filed on Sep. 6, 2005.

(51) **Int. Cl.**

G11C 5/00	(2006.01)
G11C 5/14	(2006.01)
H01L 23/10	(2006.01)
H01L 23/31	(2006.01)
H01L 23/34	(2006.01)
H03B 5/04	(2006.01)
H03B 5/36	(2006.01)
H03L 1/04	(2006.01)
H03L 7/07	(2006.01)
H03L 7/099	(2006.01)
H03L 7/197	(2006.01)
H01L 23/522	(2006.01)
H03L 7/089	(2006.01)

(52) **U.S. Cl.**

CPC ***H03B 5/36*** (2013.01); ***H03L 1/027*** (2013.01); ***H03L 1/04*** (2013.01); ***H03L 7/07*** (2013.01); ***H03L 7/099*** (2013.01); ***H03L 7/1976*** (2013.01); *H01L 23/5227* (2013.01); *H01L 2224/48247* (2013.01); *H01L 2224/49175* (2013.01); *H01L 2924/19041* (2013.01); *H01L 2924/3011* (2013.01); *H01L 2924/30107* (2013.01); *H03L 7/0891* (2013.01)

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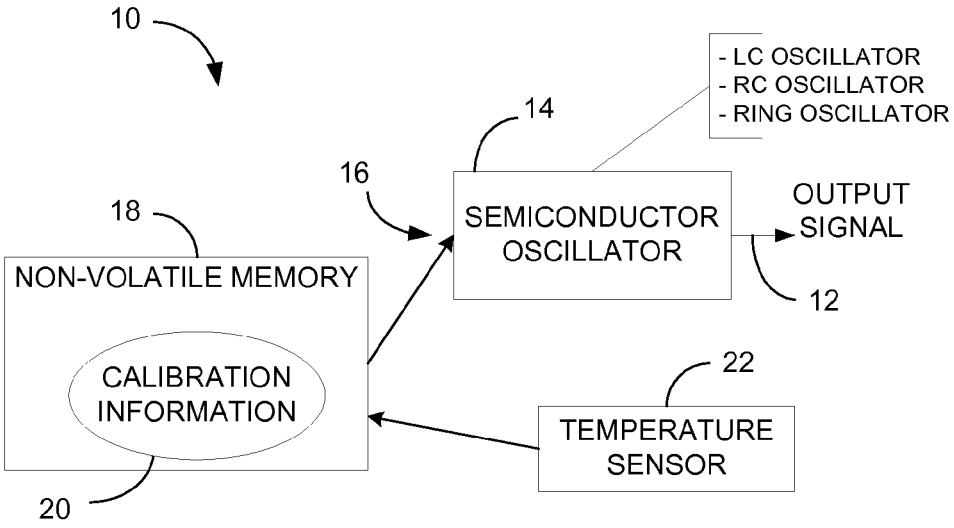

FIG. 1

30

Temperature Change (C)	Correction Factor
100	1.48
90	
80	
70	
60	1.21
.	
.	
.	
10	0.92
0	
-10	
-20	0.83

FIG. 2

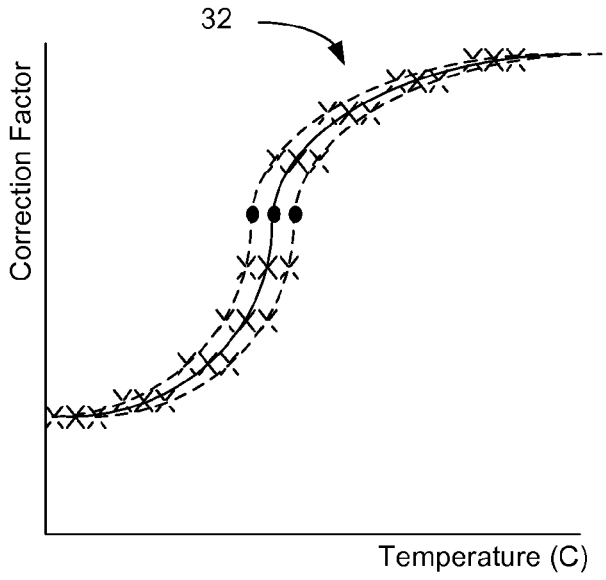

FIG. 3

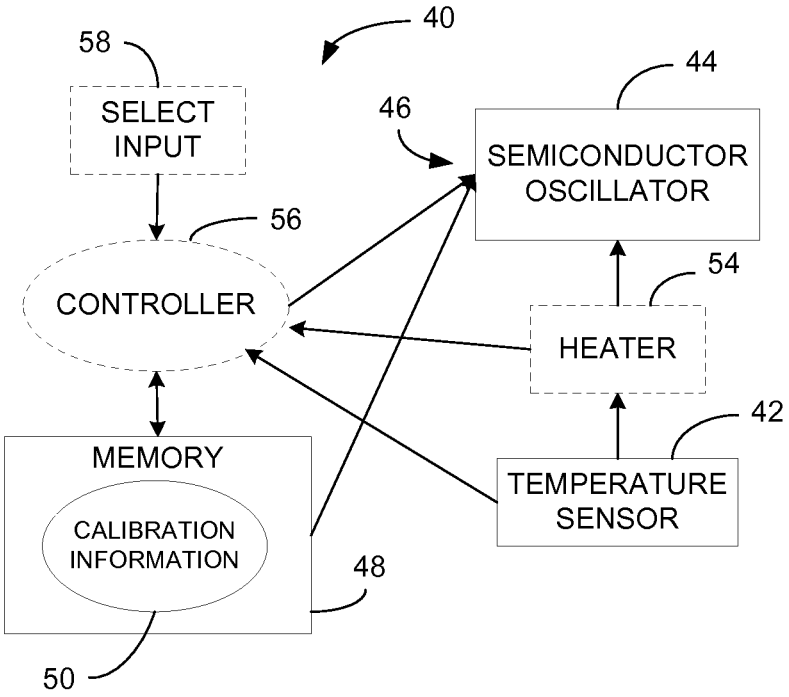
40
58
SELECT INPUT
46
44
SEMICONDUCTOR OSCILLATOR
56
CONTROLLER
54
HEATER
42
MEMORY
CALIBRATION INFORMATION
TEMPERATURE SENSOR
48
50

FIG. 4

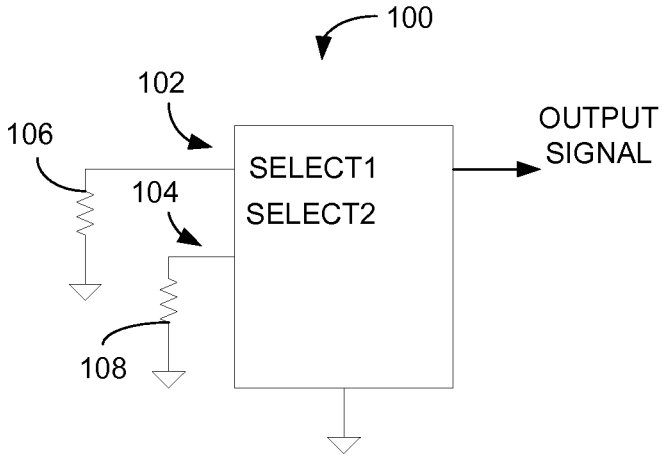
100
102
106
SELECT1
SELECT2
OUTPUT SIGNAL
104
108

FIG. 5

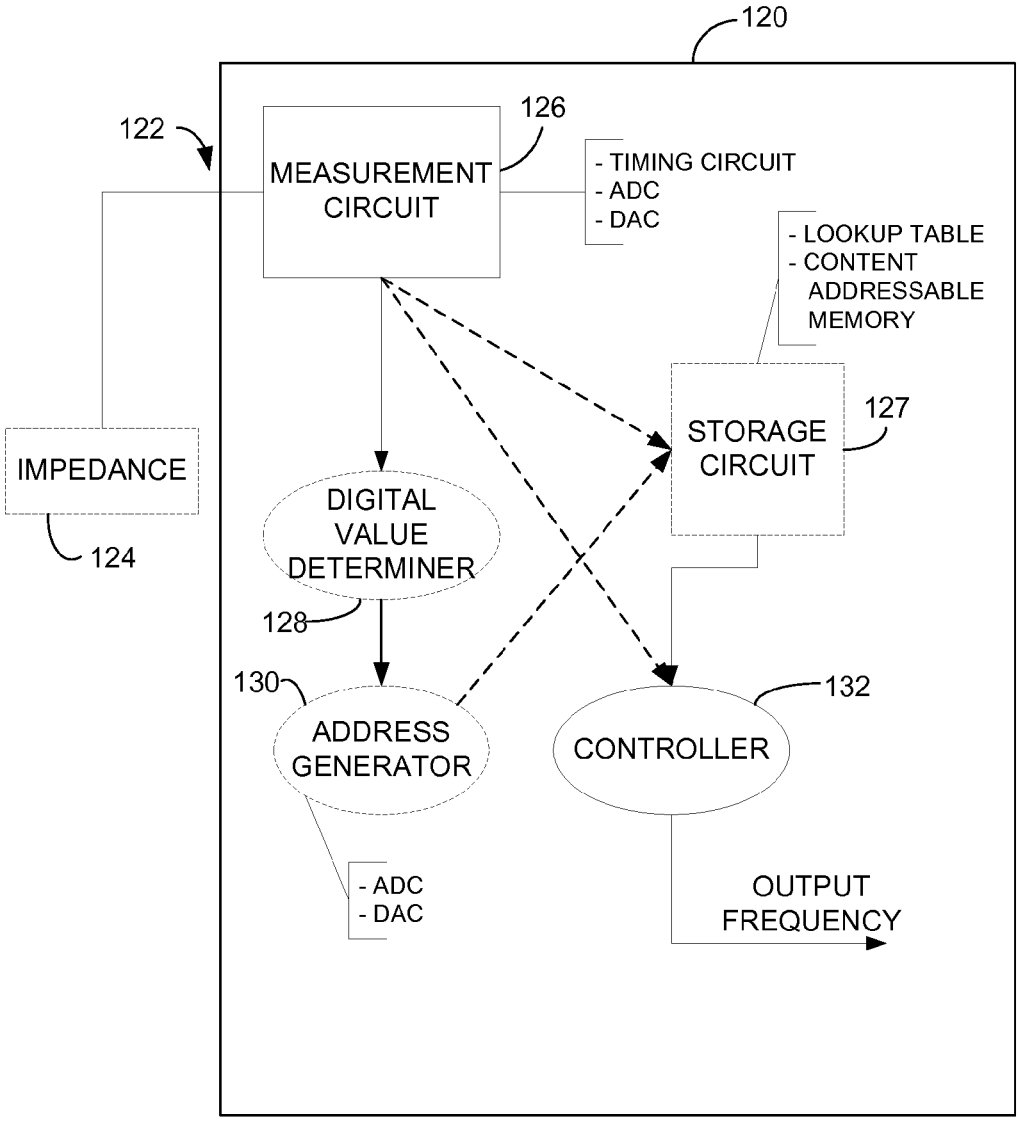
120
122
126
MEASUREMENT CIRCUIT
- TIMING CIRCUIT
- ADC
- DAC
- LOOKUP TABLE
- CONTENT ADDRESSABLE MEMORY
STORAGE CIRCUIT
127
IMPEDANCE
124
DIGITAL VALUE DETERMINER
128
130
ADDRESS GENERATOR
CONTROLLER
132
- ADC
- DAC
OUTPUT FREQUENCY

FIG. 6

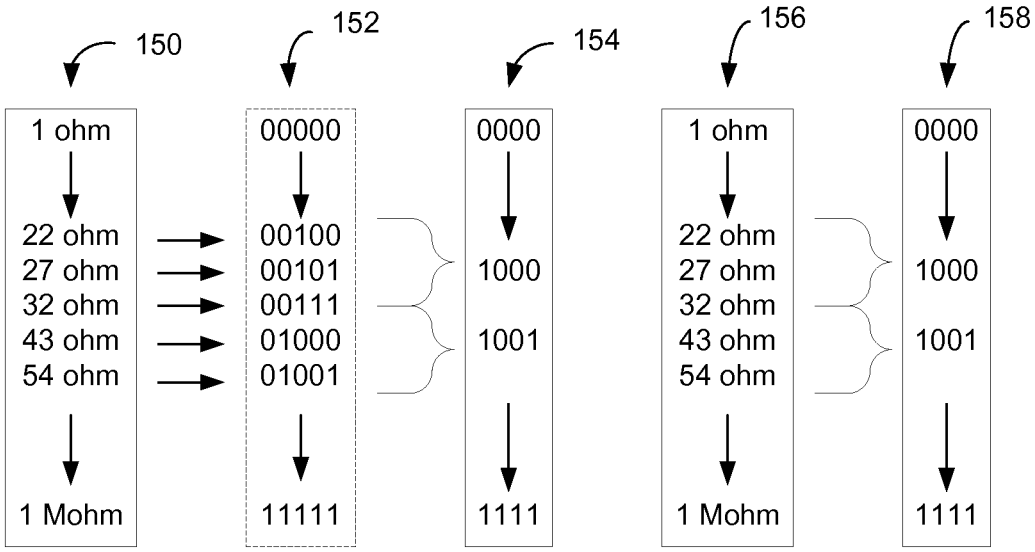

FIG. 7A FIG. 7B

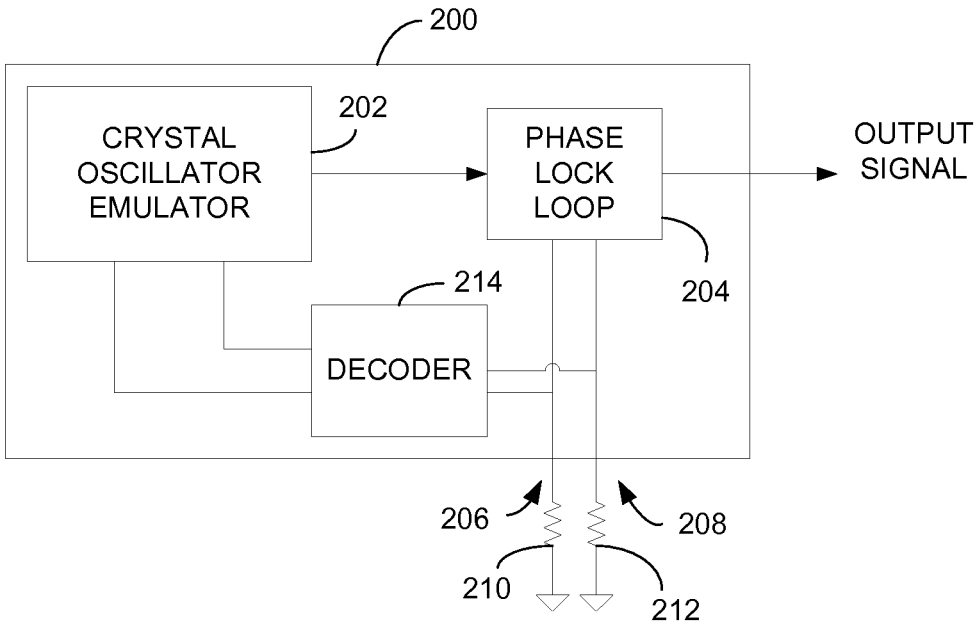

FIG. 8

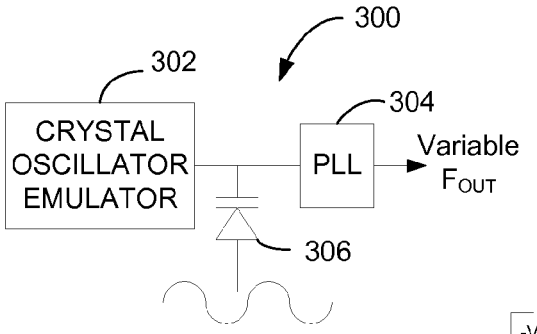

FIG. 9

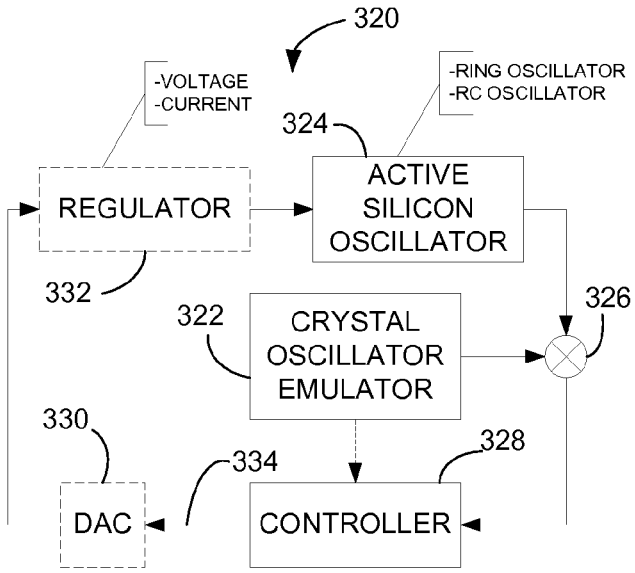

FIG. 11

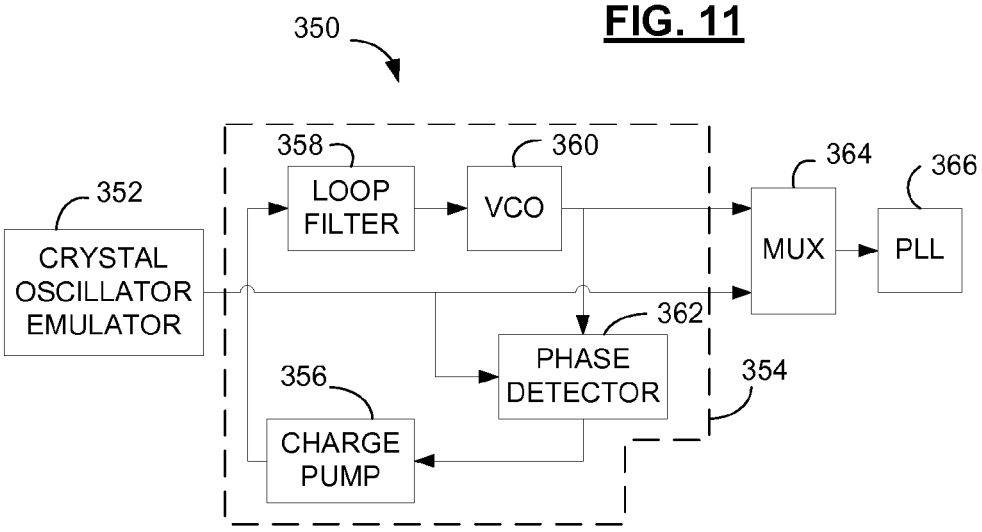

FIG. 12

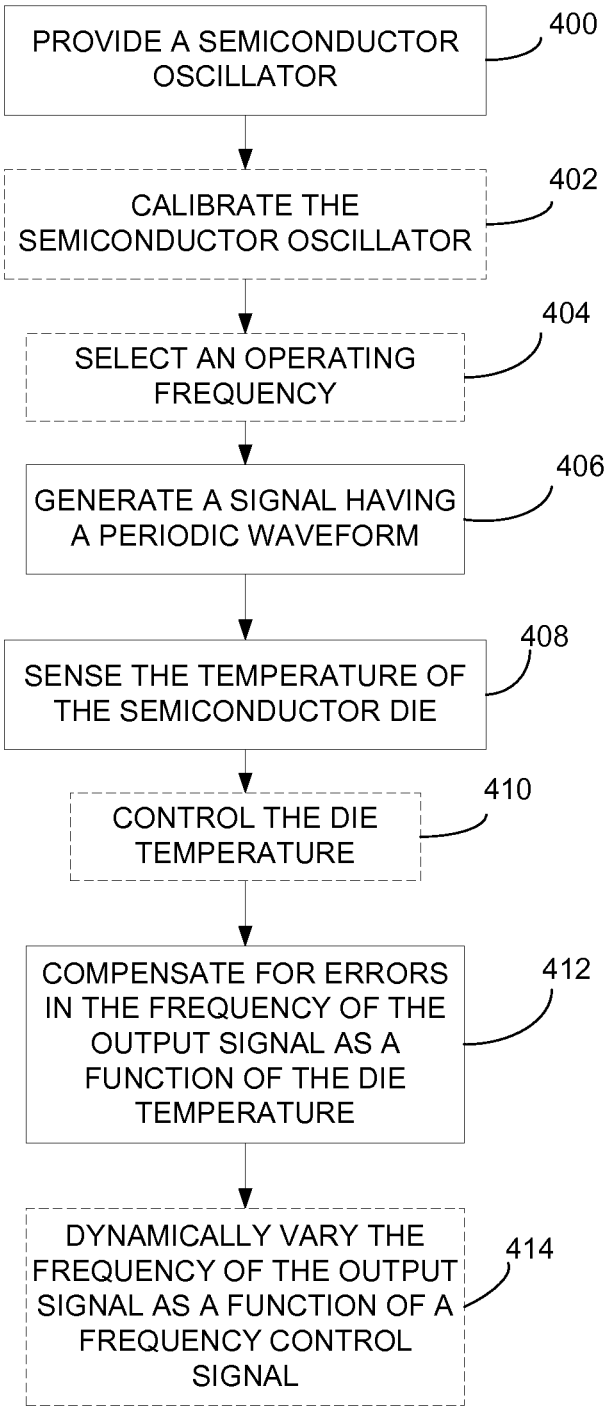
PROVIDE A SEMICONDUCTOR OSCILLATOR
400
CALIBRATE THE SEMICONDUCTOR OSCILLATOR
402
SELECT AN OPERATING FREQUENCY
404
GENERATE A SIGNAL HAVING A PERIODIC WAVEFORM
406
SENSE THE TEMPERATURE OF THE SEMICONDUCTOR DIE
408
CONTROL THE DIE TEMPERATURE
410
COMPENSATE FOR ERRORS IN THE FREQUENCY OF THE OUTPUT SIGNAL AS A FUNCTION OF THE DIE TEMPERATURE
412
DYNAMICALLY VARY THE FREQUENCY OF THE OUTPUT SIGNAL AS A FUNCTION OF A FREQUENCY CONTROL SIGNAL
414

FIG. 10

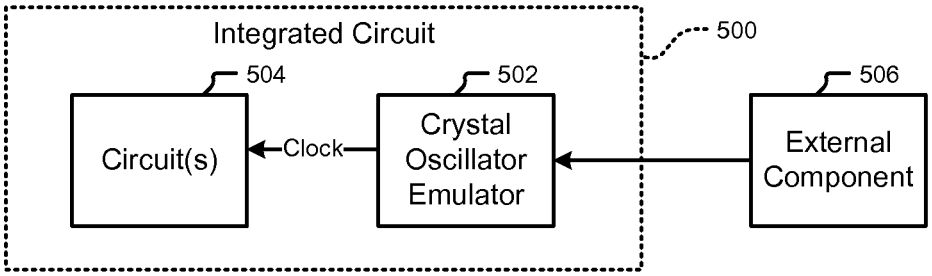

FIG. 13

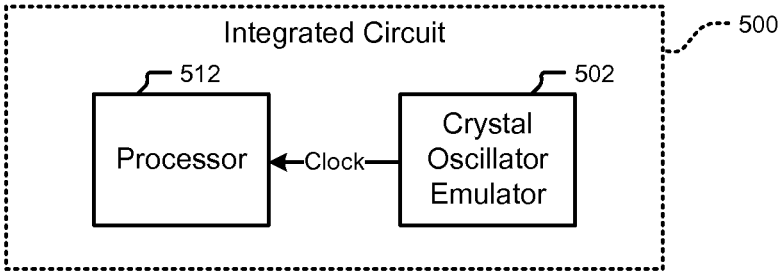

FIG. 14

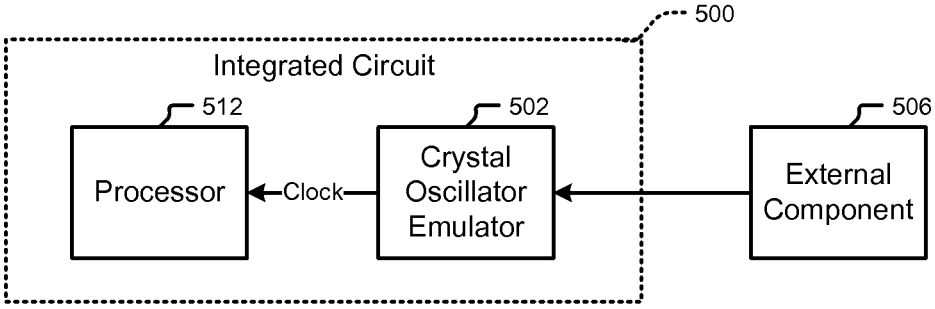

FIG. 15

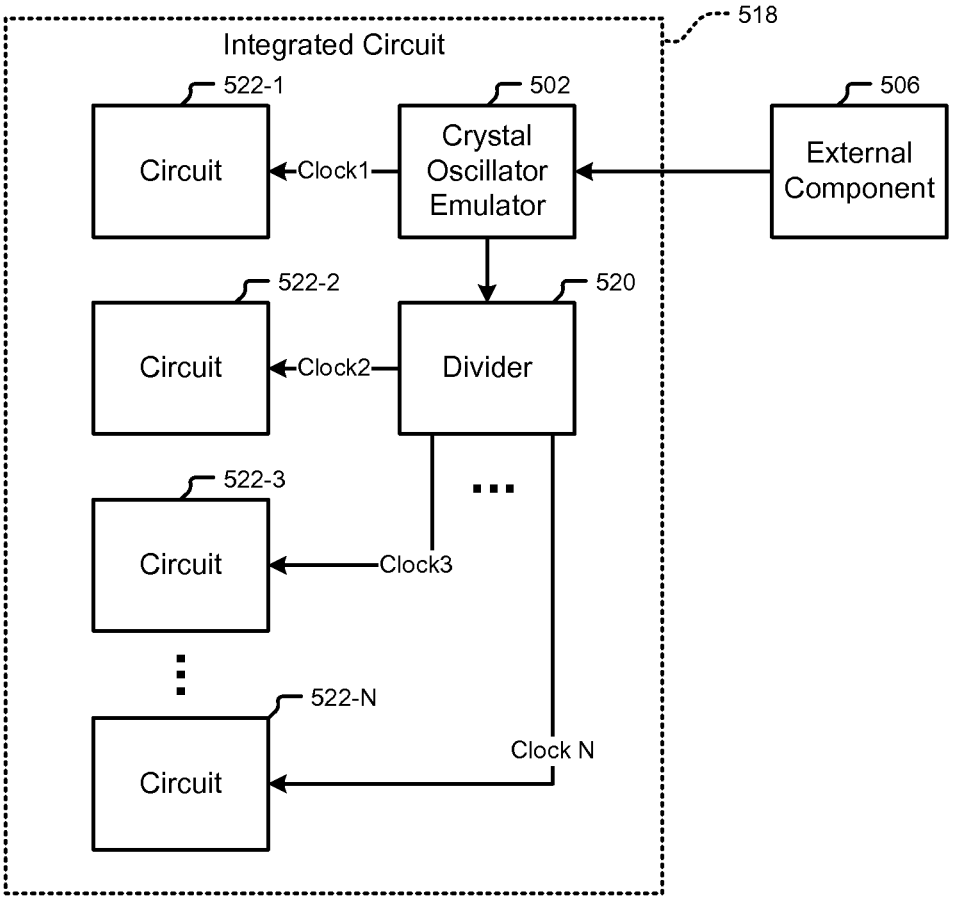
518
Integrated Circuit
522-1
502
506
Circuit
Clock1
Crystal Oscillator Emulator
External Component
522-2
520
Circuit
Clock2
Divider
522-3
Circuit
Clock3
522-N
Clock N
Circuit

FIG. 16

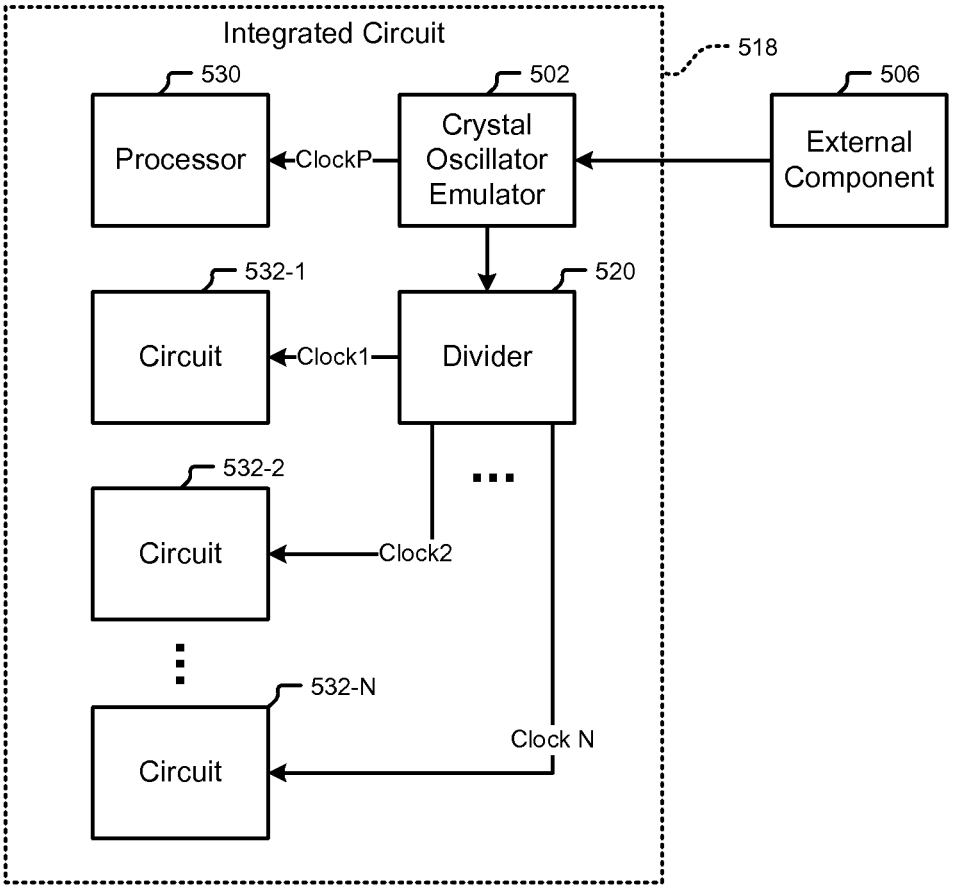
Integrated Circuit
518
530
502
506
Processor
ClockP
Crystal Oscillator Emulator
External Component
532-1
520
Circuit
Clock1
Divider
532-2
Circuit
Clock2
532-N
Circuit
Clock N

FIG. 17

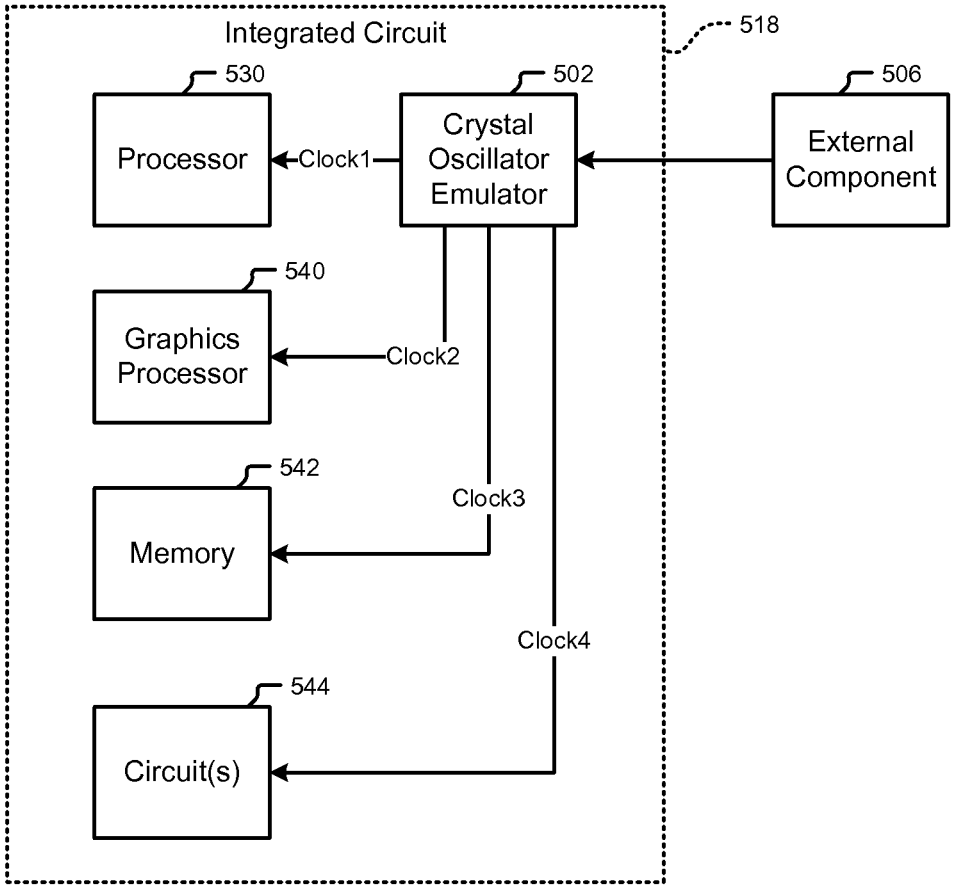
Integrated Circuit
518
530
502
506
Processor
Clock1
Crystal Oscillator Emulator
External Component
540
Graphics Processor
Clock2
542
Clock3
Memory
Clock4
544
Circuit(s)

FIG. 18

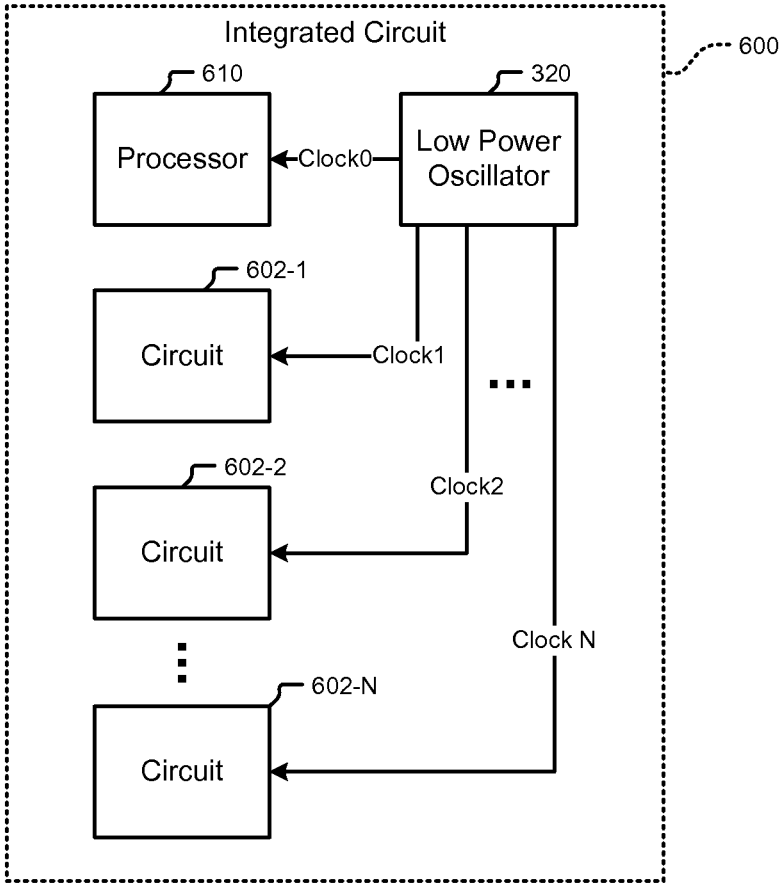
Integrated Circuit
600
610
320
Processor
Clock0
Low Power Oscillator
602-1
Circuit
Clock1
602-2
Circuit
Clock2
Clock N
602-N
Circuit

FIG. 19

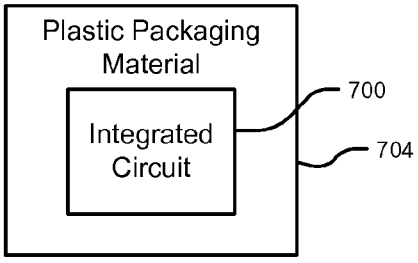

FIG. 20
Prior Art

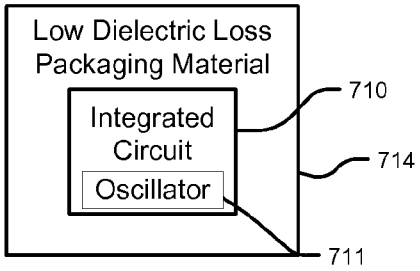

FIG. 21

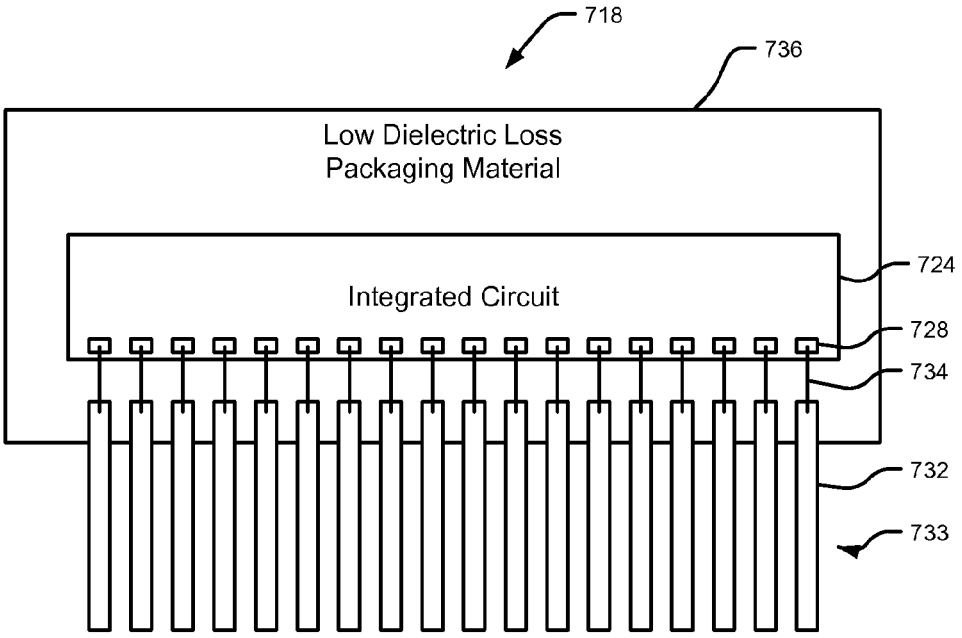

FIG. 22

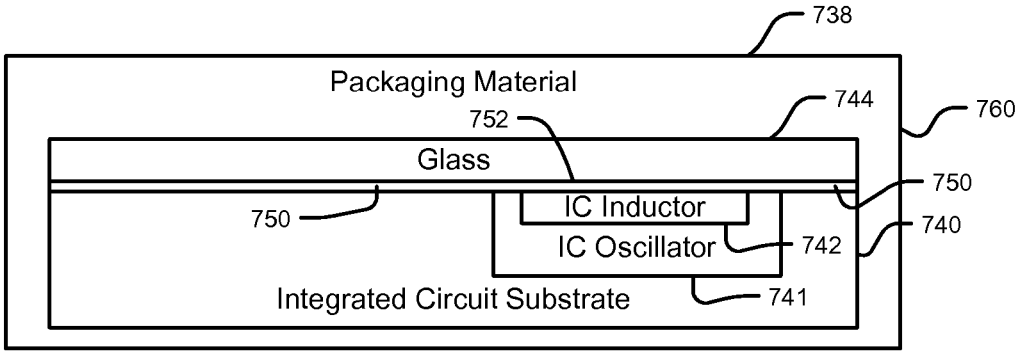

FIG. 23

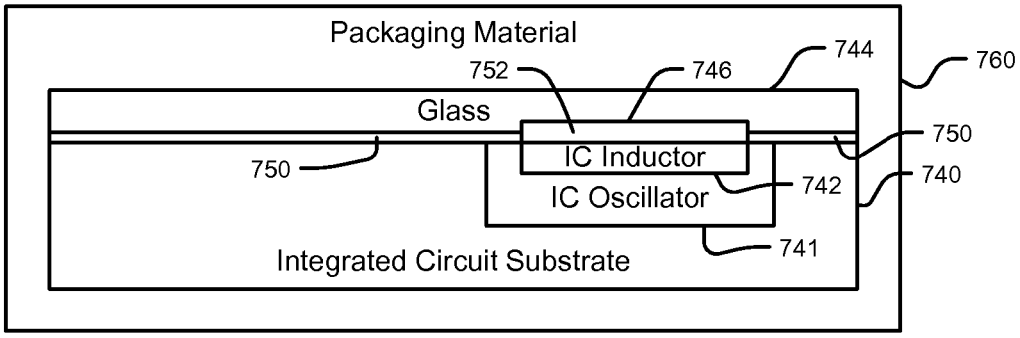

FIG. 24

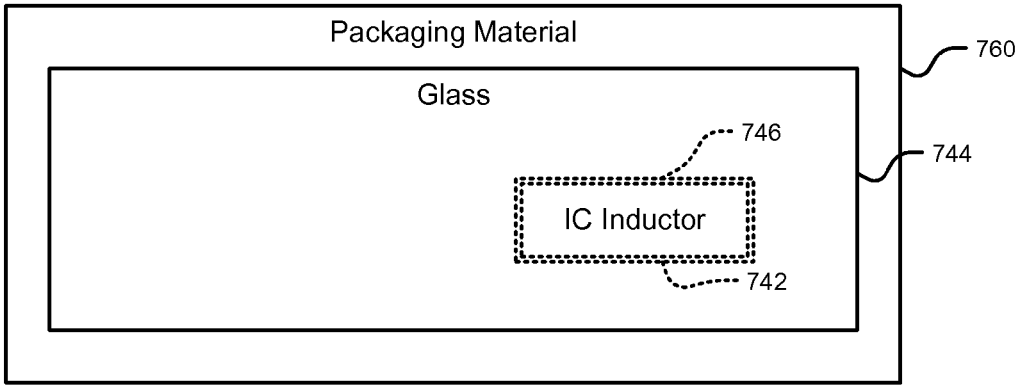

FIG. 25

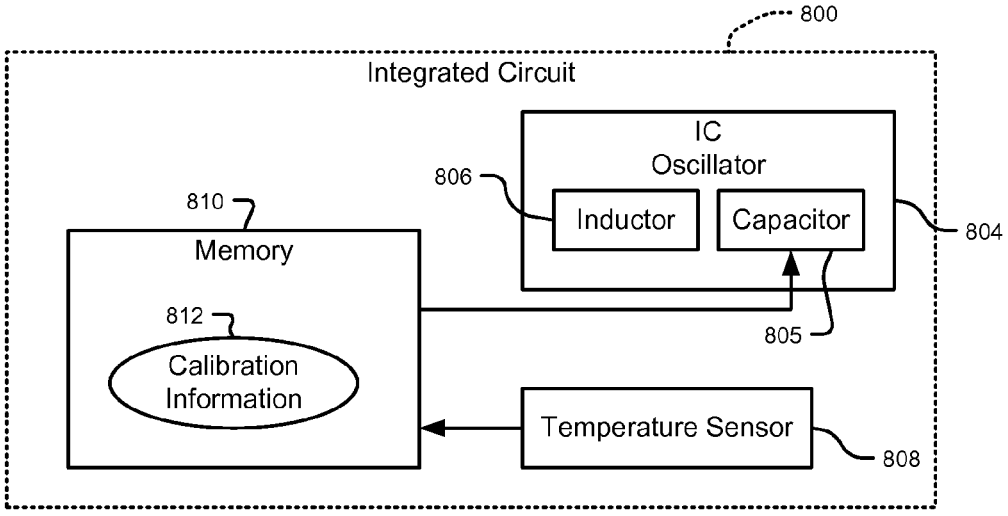
800
Integrated Circuit
IC
Oscillator
806
Inductor
Capacitor
804
810
Memory
812
Calibration
Information
805
Temperature Sensor
808

FIG. 26

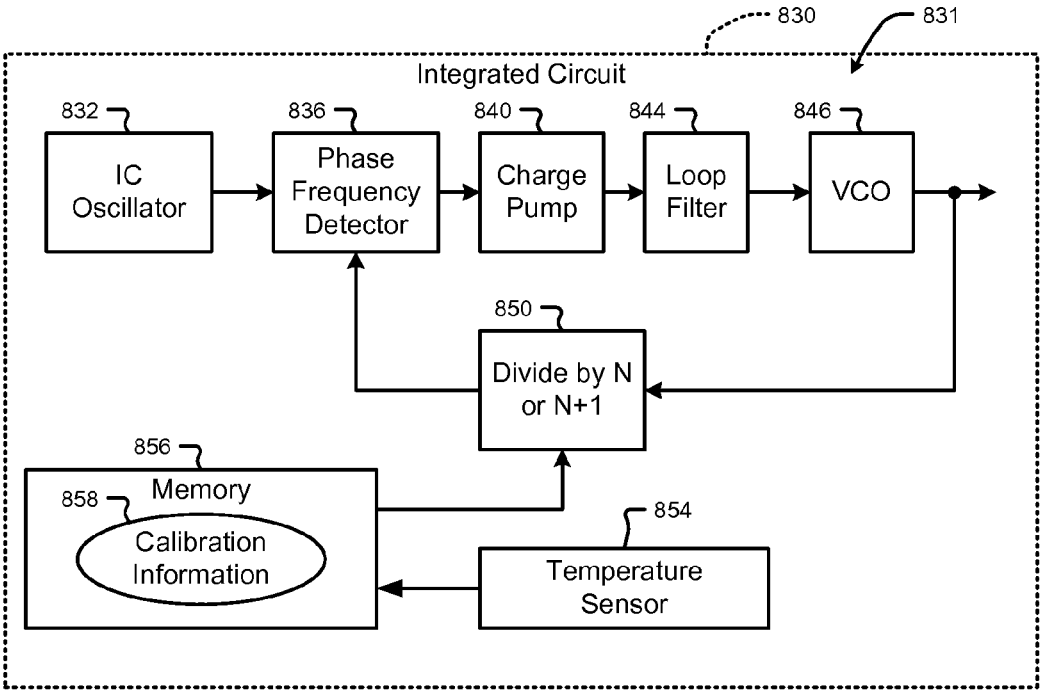
830
831
Integrated Circuit
832
IC
Oscillator
836
Phase
Frequency
Detector
840
Charge
Pump
844
Loop
Filter
846
VCO
850
Divide by N
or N+1
856
Memory
858
Calibration
Information
854
Temperature
Sensor

FIG. 27

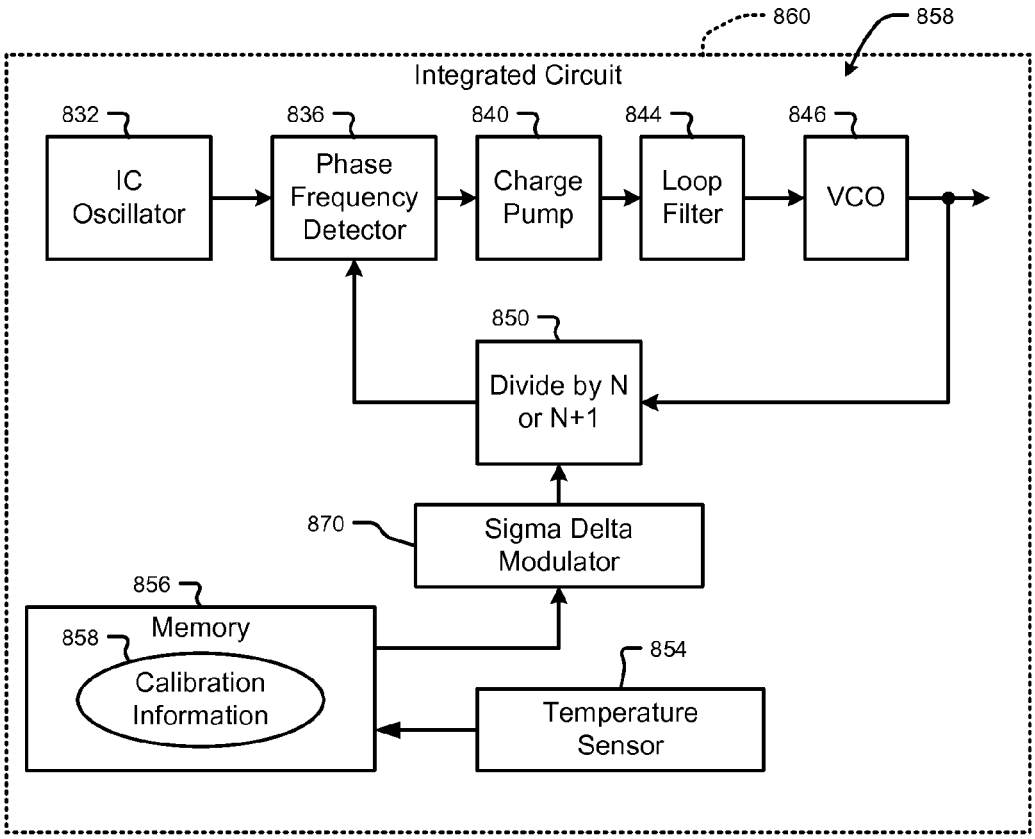
860
858
Integrated Circuit
832
IC Oscillator
836
Phase Frequency Detector
840
Charge Pump
844
Loop Filter
846
VCO
850
Divide by N or N+1
870
Sigma Delta Modulator
856
Memory
858
Calibration Information
854
Temperature Sensor

FIG. 28

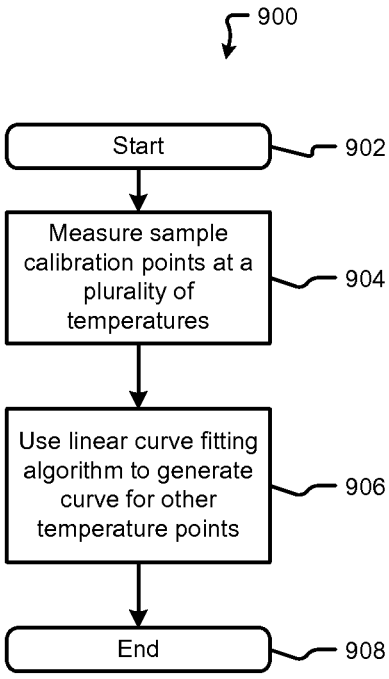
900
Start
902
Measure sample calibration points at a plurality of temperatures
904
Use linear curve fitting algorithm to generate curve for other temperature points
906
End
908

FIG. 29

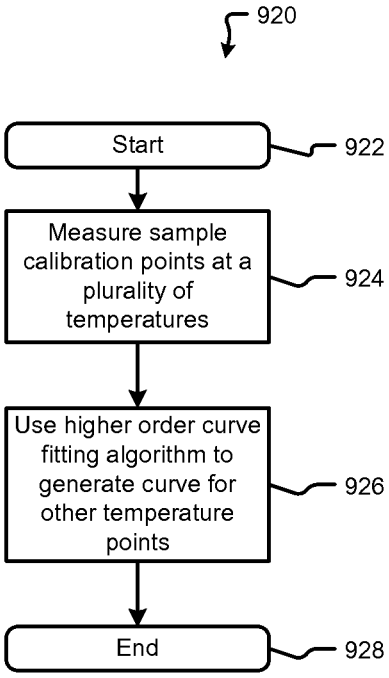
920
Start
922
Measure sample calibration points at a plurality of temperatures
924
Use higher order curve fitting algorithm to generate curve for other temperature points
926
End
928

FIG. 30

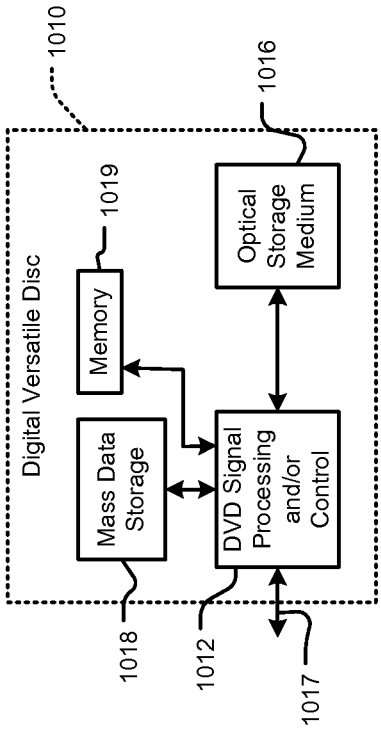

FIG. 31B

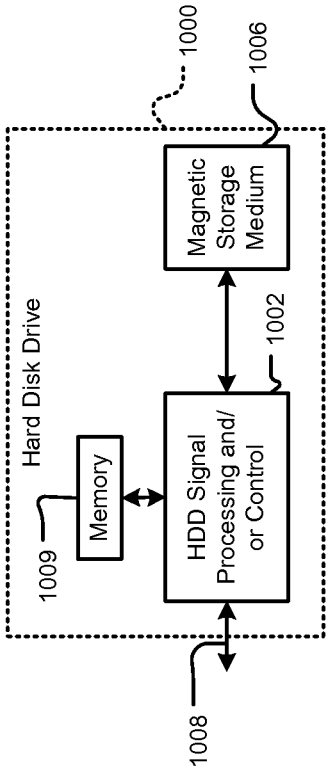

FIG. 31A

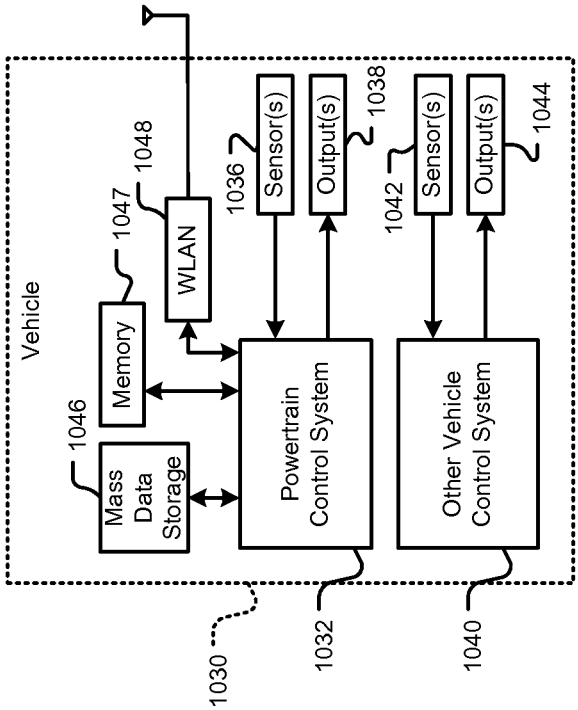

FIG. 31D

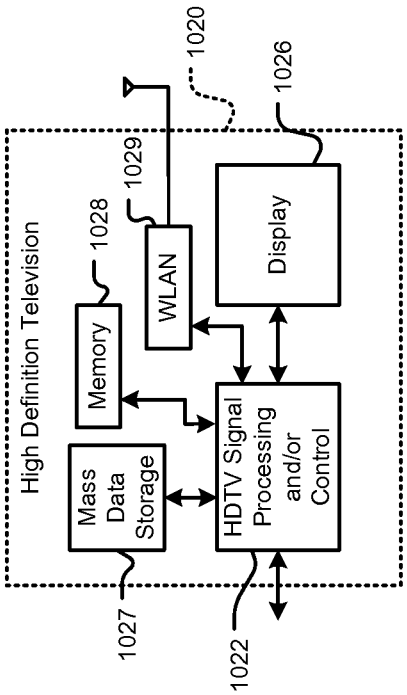

FIG. 31C

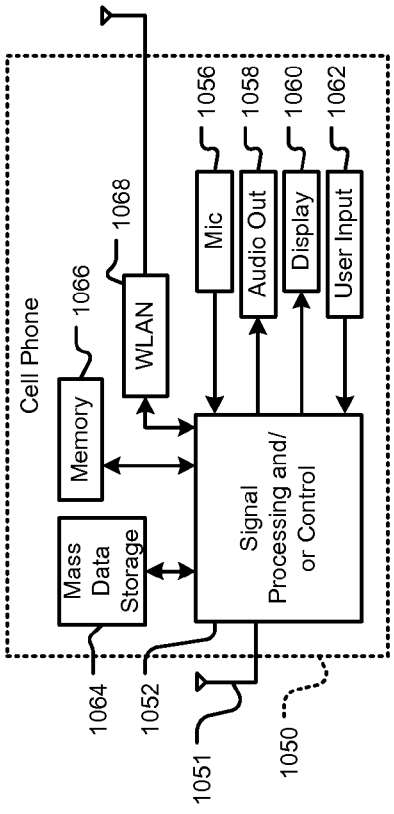

FIG. 31E

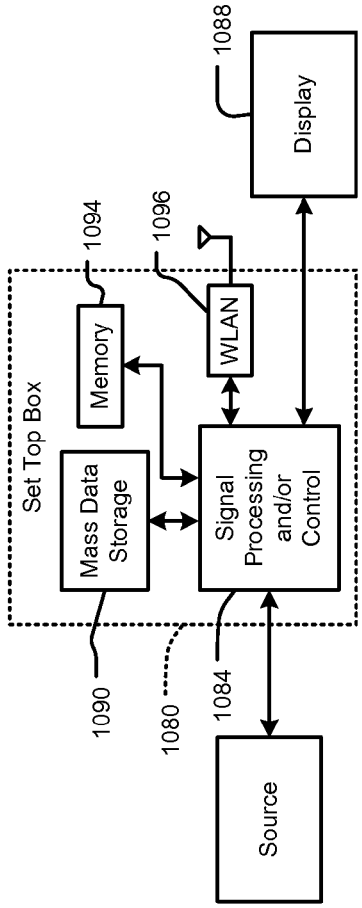

FIG. 31F

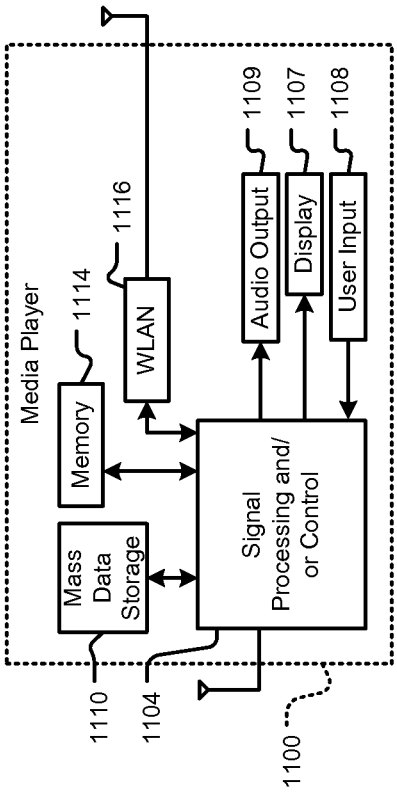
Media Player
Memory
1114
Mass Data Storage
WLAN
1116
Signal Processing and/or Control
Audio Output
1109
Display
1107
User Input
1108
1110
1104
1100

FIG. 31G

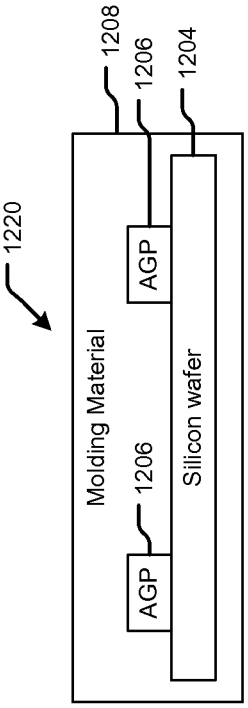

FIG. 32C

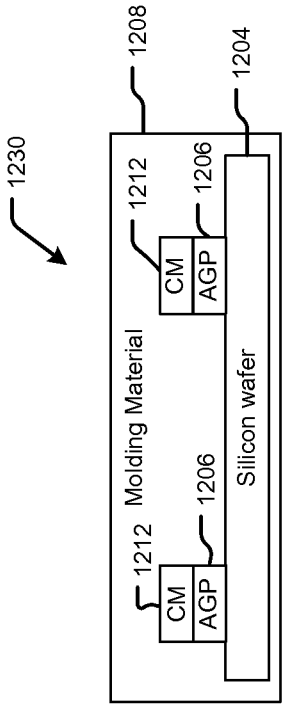

FIG. 32D

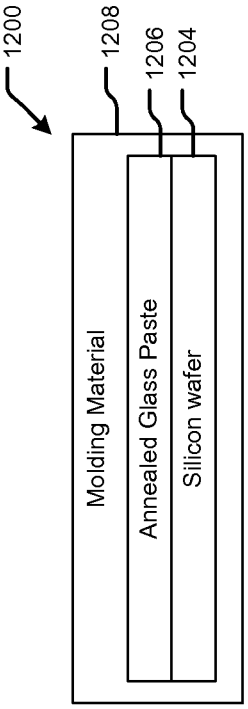

FIG. 32A

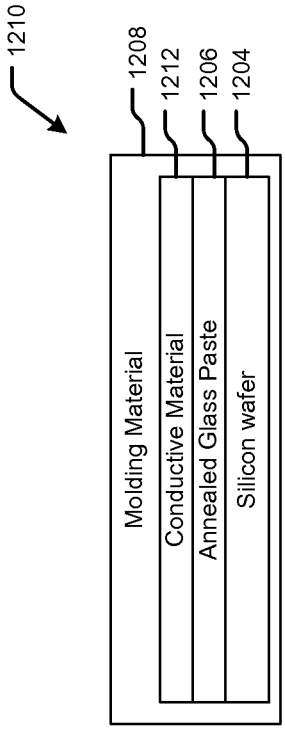

FIG. 32B

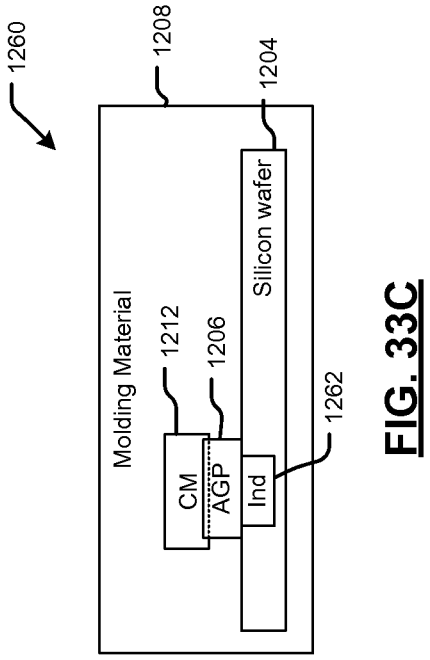

FIG. 33C

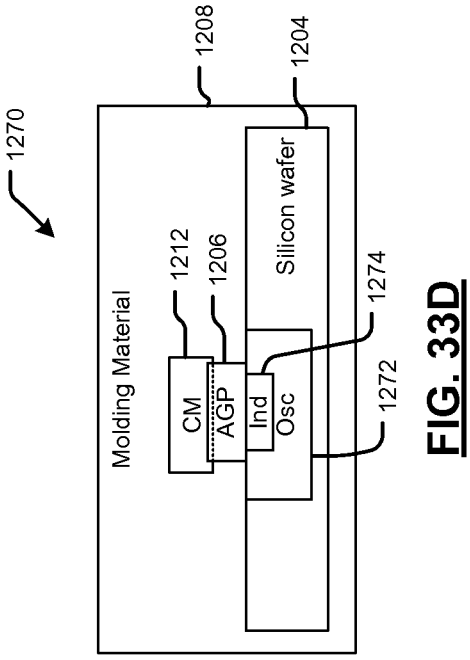

FIG. 33D

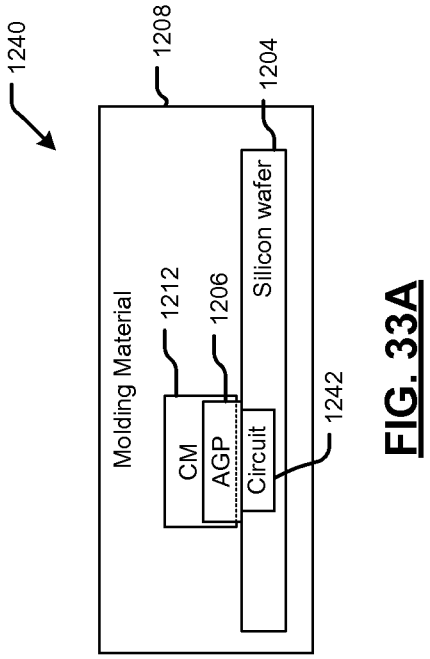

FIG. 33A

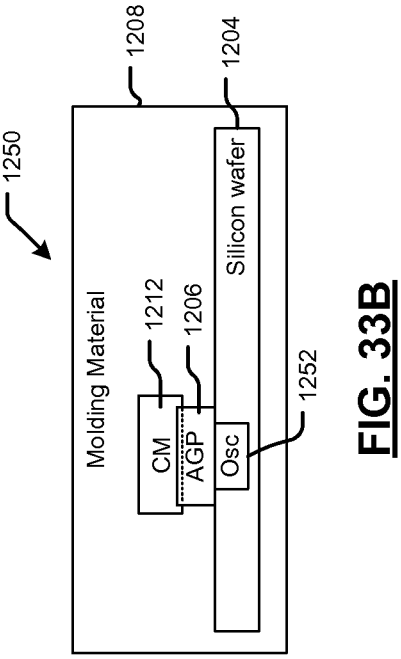

FIG. 33B

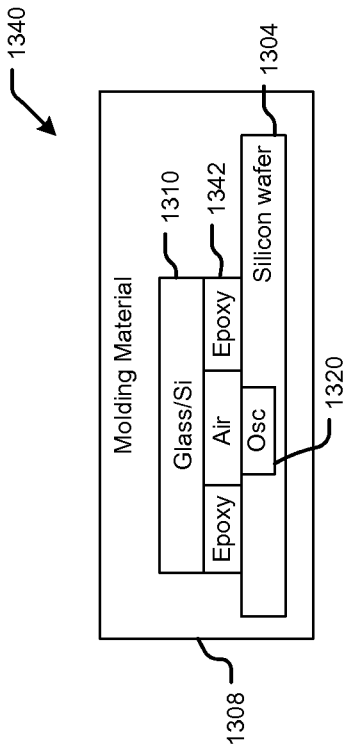

FIG. 34C

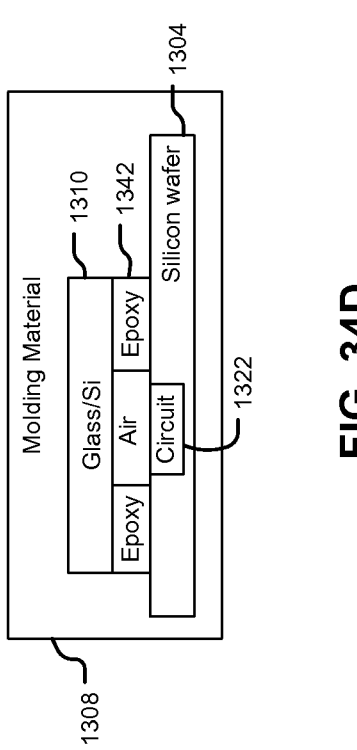

FIG. 34D

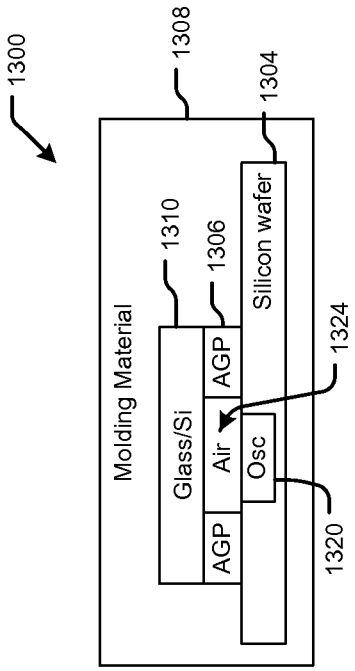

FIG. 34A

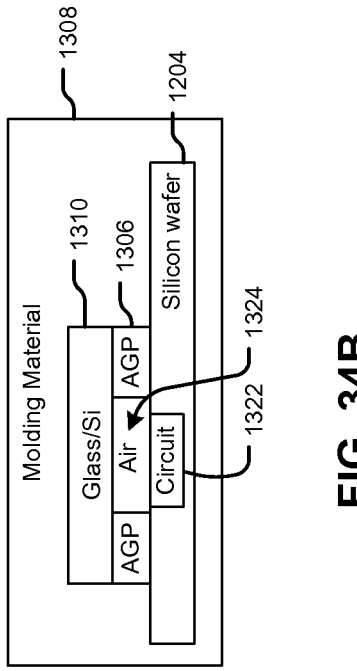

FIG. 34B

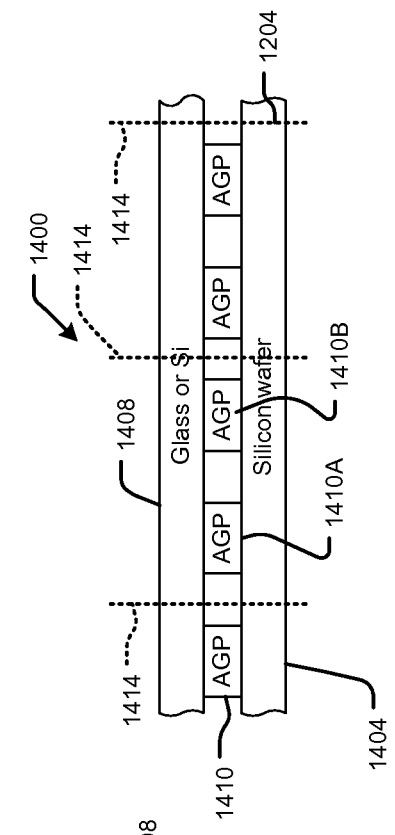

FIG. 36A

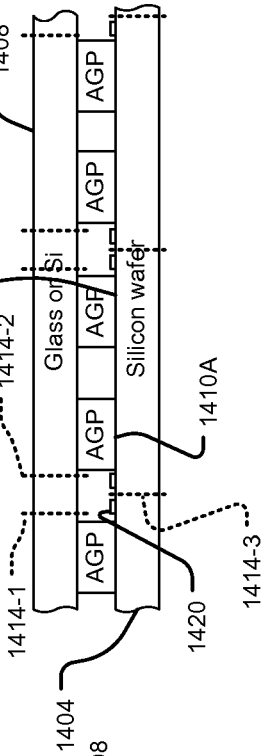

FIG. 36B

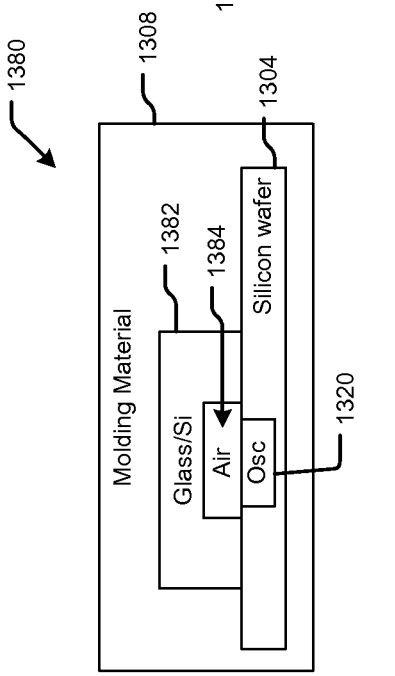

FIG. 35A

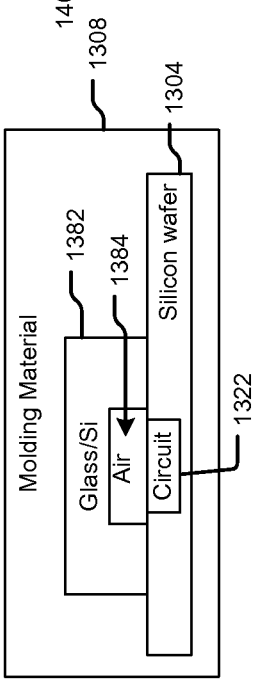

FIG. 35B

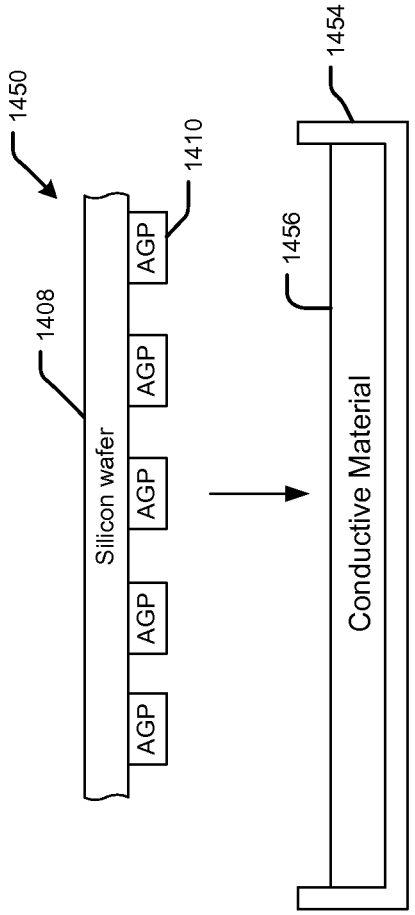

FIG. 37A

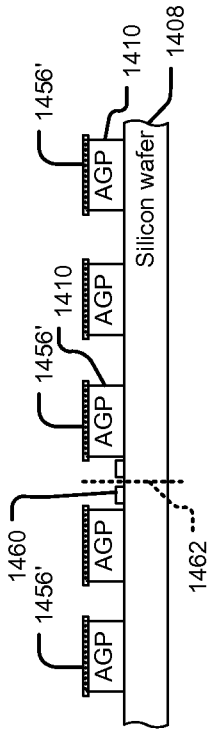

FIG. 37B

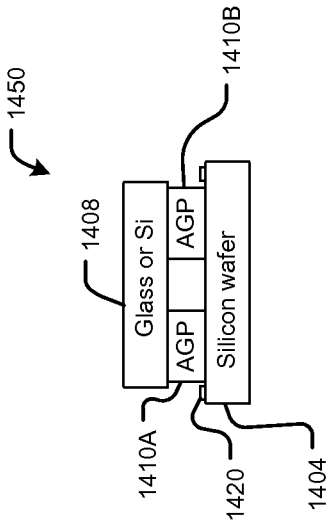

FIG. 36C

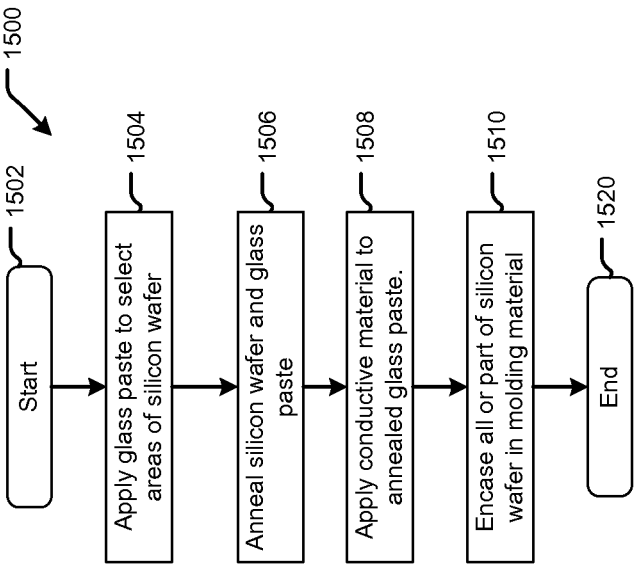
1500
1502
Start
1504
Apply glass paste to select areas of silicon wafer
1506
Anneal silicon wafer and glass paste
1508
Apply conductive material to annealed glass paste.
1510
Encase all or part of silicon wafer in molding material
1520
End

FIG. 38

SYSTEMS AND METHODS FOR CONFIGURING A SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

The present disclosure is a continuation U.S. patent application Ser. No. 14/089,261 (now U.S. Pat. No. 9,143,083), filed Nov. 25, 2013, which is a continuation of U.S. patent application Ser. No. 11/486,557, filed Jul. 14, 2006, which is a continuation of U.S. patent application Ser. No. 11/328,979, filed Jan. 10, 2006, which claims the benefit of U.S. Provisional Application No. 60/756,828, filed Jan. 6, 2006, U.S. Provisional Application No. 60/730,568, filed Oct. 27, 2005, and U.S. Provisional Application No. 60/714,454, filed Sep. 6, 2005, and is a continuation-in-part of U.S. patent application Ser. No. 10/892,709 (now U.S. Pat. No. 7,148,763), filed Jul. 16, 2004, which is a continuation-in-part of U.S. patent application Ser. No. 10/272,247 (now U.S. Pat. No. 7,042,301), filed Oct. 15, 2002. The entire disclosures of the applications referenced above are incorporated herein by reference.

FIELD

This invention relates to integrated circuits, and more particularly to integrated circuits with annealed glass paste arranged on a silicon wafer.

BACKGROUND

Precision frequency references are required in many types of electronic devices such as cellular phones and other handheld devices. Crystal oscillators are typically used to provide the precision frequency reference in these electronic devices. However, crystal oscillators have several inherent disadvantages including large bulky size, fragility, and high cost. In addition, the size and cost of crystal oscillators is related to the resonant frequency so that as the frequency increases, the size decreases, and the cost and fragility may rapidly increase. As the size of electronic devices continues to decrease, the use of crystal oscillators becomes more problematic due to the size, fragility, and cost limitations.

Semiconductor oscillators have been a poor alternative to crystal oscillators and are generally unsuitable for use as a precision frequency reference due to excessive variation in the oscillating frequency, especially with changes in temperature.

SUMMARY

An integrated circuit (IC) package comprises a IC wafer and an annealed glass paste (AGP) layer that is arranged adjacent to the IC wafer.

In other features, a molding material encapsulates at least part of the IC wafer and the AGP layer. The AGP layer is arranged on at least one side of the IC wafer. The AGP layer is arranged on a plurality of disjoint areas on at least one side of the IC wafer. A layer of a conductive material that is arranged on a portion of the AGP layer.

In other features, the IC wafer comprises a circuit component arranged in the IC wafer. The AGP layer is arranged between the circuit component and the molding material. The circuit component comprises at least one of an oscillator and an inductor. The inductor comprises a spiral inductor. The molding material encapsulates, a portion of the IC wafer. The AGP layer comprises a glass frit. The AGP layer is arranged adjacent to the IC wafer using one of a screen printing, dipping and masking.

In other features, the conductive material comprises one of a conductive epoxy and a conductive epoxy paint. The layer of the conductive material is arranged on the AGP layer by dipping the IC package in a container containing the conductive material.

An integrated circuit comprises a temperature sensor that senses a temperature of the integrated circuit. A memory module stores data relating to oscillator calibrations and selects one of the oscillator calibrations as a function of the sensed temperature. An oscillator module generates a reference signal having a frequency. A phase locked loop module includes a feedback loop having a feedback loop parameter and selectively adjusts the feedback loop parameter based on the selected one of the oscillator calibrations.

In other features, the phase locked loop module comprises a fractional phase locked loop and the feedback loop parameter is a ratio of a scaling factor. The fractional phase locked loop comprises a phase frequency detector module that communicates with the oscillator module and that receives the reference frequency. A charge pump module communicates with the phase frequency detector module. A voltage controlled oscillator module communicates with the charge pump module and generates an output frequency. A scaling module communicates with the voltage controlled oscillator module and the phase frequency detector module, selectively adjusts the output frequency based on first and second scaling factors, and adjusts a ratio of the first and second scaling factors based on the selected one of the oscillator calibrations.

In other features, the first and second scaling factors are divisors equal to N and N+1, and wherein N is an integer greater than zero. The phase locked loop module comprises a Sigma Delta fractional phase locked loop module and the feedback loop parameter includes modulation of a scaling divisor. The Sigma Delta fractional phase locked loop module comprises a phase frequency detector module that communicates with the oscillator module and that receives the reference frequency. A charge pump module communicates with the phase frequency detector module. A voltage controlled oscillator module communicates with the charge pump module and that generates an output frequency. A scaling module communicates with the voltage controlled oscillator module and the phase frequency detector module and selectively divides the output frequency by first and second scaling factors. A Sigma Delta modulator adjusts modulation of the scaling module between the first and second scaling factors based on the selected one of the oscillator calibrations. The first and second scaling factors are divisors equal to N and N+1, where N is an integer greater than zero.

An integrated circuit comprises temperature sensing means for sensing a temperature of the integrated circuit. Memory means for storing data relating to oscillator calibrations and for selecting one of the oscillator calibrations as a function of the sensed temperature. Oscillating means generates a reference signal having a frequency based on the oscillator calibrations. Phase locked loop means, that includes a feedback loop having a feedback loop parameter, selectively adjusts the feedback loop parameter based on the selected one of the oscillator calibrations.

In other features, the phase locked loop means comprises a fractional phase locked loop and the feedback loop parameter is a ratio of a scaling factor. The fractional phase locked loop comprises phase frequency detector means, that communicates with the oscillating means, for receiving the reference frequency. Charge pump means generates voltage and com-

municates with the phase frequency detector means. Voltage controlled oscillator means, that communicates with the charge pump means, generates an output frequency. Scaling means, that communicates with the voltage controlled oscillator means and the phase frequency detector means, selectively adjusts the output frequency based on first and second scaling factors and adjusts a ratio of the first and second scaling factors based on the selected one of the oscillator calibrations.

In other features, the first and second scaling factors are divisors equal to N and N+1, and wherein N is an integer greater than zero. The phase locked loop means comprises a Sigma Delta fractional phase locked loop and the feedback loop parameter includes modulation of a scaling divisor. The Sigma Delta fractional phase locked loop comprises phase frequency detector means, that communicates with the oscillator means, for receiving the reference frequency. Charge pump means generates a voltage and communicates with the phase frequency detector means. Voltage controlled oscillator means, that communicates with the charge pump means, generates an output frequency. Scaling means, that communicates with the voltage controlled oscillator means and the phase frequency detector means, selectively divides the output frequency by first and second scaling factors. Sigma Delta modulating means adjusts modulation of the scaling means between the first and second scaling factors based on the selected one of the oscillator calibrations. The first and second scaling factors are divisors equal to N and N+1, where N is an integer greater than zero.

A method for operating an integrated circuit comprises sensing a temperature of the integrated circuit; storing data relating to oscillator calibrations; selecting one of the oscillator calibrations as a function of the sensed temperature; generating a reference signal having a frequency based on the oscillator calibrations; and selectively adjusting a feedback loop parameter of a phase locked loop based on the selected one of the oscillator calibrations.

In other features, the phase locked loop comprises a fractional phase locked loop and the feedback loop parameter is a ratio of a scaling factor. The phase locked loop comprises a Sigma Delta fractional phase locked loop and the feedback loop parameter includes modulation of a scaling divisor.

An integrated circuit package comprises an integrated circuit that comprises a temperature sensor that senses a temperature of the integrated circuit. A memory module stores data relating to oscillator calibrations and that selects one of the oscillator calibrations as a function of the sensed temperature. An oscillator module generates a reference signal having a frequency that is based on the selected one of the oscillator calibrations. A packaging material encases at least part of the integrated circuit and has a low dielectric loss.

In other features, the packaging material includes at least one material selected from a group consisting of polychlorotrifluoroethylene, fluorinated ethylene propylene copolymer, perfluoroalkoxy, and a copolymer of ethylene and tetrafluoroethylene. The packaging material includes a low dielectric loss plastic.

An integrated circuit package comprises an integrated circuit that comprises an oscillator module that generates a reference signal having a frequency that is based on one of a plurality of oscillator calibration settings. A packaging material encases at least part of the integrated circuit and has a low dielectric loss.

In other features, the integrated circuit further comprises a temperature sensor that senses a temperature of the integrated circuit. A memory module stores the oscillator calibration settings. The packaging material includes at least one material selected from a group consisting of polychlorotrifluoroethylene, fluorinated ethylene propylene copolymer, perfluoroalkoxy, and a copolymer of ethylene and tetrafluoroethylene. The packaging material includes a low dielectric loss plastic.

A method for providing an integrated circuit package comprises providing an integrated circuit; encasing the integrated circuit in a packaging material that has a low dielectric loss; sensing a temperature of the integrated circuit during operation; storing data relating to oscillator calibrations; selecting one of the oscillator calibrations as a function of the sensed temperature; and generating a reference signal having a frequency that is based on the selected one of the oscillator calibrations.

In other features, the packaging material includes at least one material selected from a group consisting of polychlorotrifluoroethylene, fluorinated ethylene propylene copolymer, perfluoroalkoxy, and a copolymer of ethylene and tetrafluoroethylene. The packaging material includes a low dielectric loss plastic.

A method for providing an integrated circuit package comprises providing an integrated circuit; selecting one of a plurality of oscillator calibration settings; generating a reference signal having a frequency that is based on the one of the plurality of oscillator calibration settings; and encasing the integrated circuit in a packaging material that has a low dielectric loss.

In other features, the method comprises sensing a temperature of the integrated circuit; and selecting the one of the plurality of oscillator calibration settings based on the sensed temperature. The packaging material includes at least one material selected from a group consisting of polychlorotrifluoroethylene, fluorinated ethylene propylene copolymer, perfluoroalkoxy, and a copolymer of ethylene and tetrafluoroethylene. The packaging material includes a low dielectric loss plastic.

An integrated circuit package comprises an integrated circuit that comprises temperature sensing means for sensing a temperature of the integrated circuit. Storing means stores data relating to oscillator calibrations and for selecting one of the oscillator calibrations as a function of the sensed temperature. Oscillating means generates a reference signal having a frequency that is based on the selected one of the oscillator calibrations. Packaging means encases at least part of the integrated circuit and having a low dielectric loss.

In other features, the packaging means includes at least one material selected from a group consisting of polychlorotrifluoroethylene, fluorinated ethylene propylene copolymer, perfluoroalkoxy, and a copolymer of ethylene and tetrafluoroethylene. The packaging means includes a low dielectric loss plastic.

An integrated circuit package comprises an integrated circuit that comprises oscillating means for generating a reference signal having a frequency that is based on one of a plurality of oscillator calibrations settings and packaging means for encasing at least part of the integrated circuit and having a low dielectric loss.

In other features, the integrated circuit further comprises temperature sensing means for sensing a temperature of the integrated circuit. Storing means stores oscillator calibration data. The packaging means includes at least one material selected from a group consisting of polychlorotrifluoroethylene, fluorinated ethylene propylene copolymer, perfluoroalkoxy, and a copolymer of ethylene and tetrafluoroethylene. The packaging means includes a low dielectric loss plastic.

An integrated circuit package comprises an integrated circuit that comprises a temperature sensor that senses a tem-

perature of the integrated circuit and a memory module that stores oscillator calibrations and that selects one of the oscillator calibrations as a function of the sensed temperature. An oscillator module generates a reference signal having a frequency that is based on the selected one of the oscillator calibrations. An epoxy layer adheres a glass layer to the integrated circuit. A packaging material encases at least part of the glass layer and the integrated circuit.

In other features, the glass layer is located between adjacent to portions of the integrated circuit that include the oscillator module. The oscillator module includes an on-chip inductor and wherein the glass layer is located adjacent to portions of the integrated circuit that include on-chip inductor. The glass layer includes a cavity that defines an air gap and wherein the cavity is adjacent to portions of the integrated circuit that include the oscillator module. The glass layer includes a cavity that defines an air gap and wherein the cavity is adjacent to portions of the integrated circuit that include an inductor of the oscillator module.

An integrated circuit package comprises an integrated circuit that comprises temperature sensing means for sensing a temperature of the integrated circuit and storing means for storing oscillator calibrations and for selecting one of the oscillator calibrations as a function of the sensed temperature. Oscillating means generates a reference signal having a frequency that is based on the selected one of the oscillating means calibrations. Means attaches a glass layer to the integrated circuit. Packaging means encases at least part of the glass layer and the integrated circuit.

In other features, the glass layer is located adjacent to portions of the integrated circuit that include the oscillating means. The oscillating means includes an on-chip inductor and wherein the glass layer is located adjacent to portions of the integrated circuit that include on-chip inductor. The glass layer includes a cavity that defines an air gap and wherein the cavity is adjacent to portions of the integrated circuit that include the oscillating means. The glass layer includes a cavity that defines an air gap and wherein the cavity is adjacent to portions of the integrated circuit that include an inductor of the oscillating means.

A method for providing an integrated circuit package comprises sensing a temperature of an integrated circuit; storing oscillator calibrations; selecting one of the oscillator calibrations as a function of the sensed temperature; generating a reference signal having a frequency that is based on the selected one of the oscillator calibrations; and attaching a glass layer to the integrated circuit; and encasing at least part of the glass layer and the integrated circuit in a packaging material.

In other features, the method includes locating the glass layer adjacent to portions of the integrated circuit that include the oscillator module. The oscillator module includes an on-chip inductor and further comprising locating the glass layer adjacent to portions of the integrated circuit that include on-chip inductor. The glass layer includes a cavity that defines an air gap and further comprising locating the cavity adjacent to portions of the integrated circuit that include the oscillator. The glass layer includes a cavity that defines an air gap and further comprising locating the cavity adjacent to portions of the integrated circuit that include an inductor of the oscillator.

An integrated circuit (IC) package comprises an IC wafer. A first portion is arranged adjacent to the IC wafer. A second portion is arranged adjacent to the IC wafer and is spaced from the first portion. The first and second portions comprise at least one of annealed glass paste (AGP) and epoxy. A layer is arranged adjacent to the first and second portions and creates an air gap between the layer, the first and second portions and the IC wafer.

In other features, the IC wafer comprises a silicon wafer. A molding material encapsulates at least part of the IC wafer, the layer and the first and second portions. The layer comprises at least one of glass and silicon. A conductive material is arranged adjacent to the first and second portions. The silicon wafer comprises a circuit component. The air gap is arranged between the circuit component, the layer and the first and second portions. The circuit component comprises at least one of an oscillator and an inductor. The inductor comprises a spiral inductor.

In other features, the first and second portions comprise glass frit. The first and second portions are applied to the silicon wafer using one of a screen printing, dipping and masking. The conductive material comprises one of a conductive epoxy and conductive epoxy paint. The conductive material is applied to the first and second portions by dipping the at least part of the IC package in a container containing the conductive material. The layer has a first width that is less than a second width of the silicon wafer. The IC wafer comprises bond pads. The layer has a first width that is less than a second width of the silicon wafer and further comprising bond pads that are located in an outer region of the silicon wafer.

A method of providing an integrated circuit (IC) package, comprises providing an IC wafer; arranging a first portion adjacent to the IC wafer; arranging a second portion adjacent to the IC wafer and spaced from the first portion, wherein the first and second portions comprise at least one of annealed glass paste (AGP) and epoxy; and arranging a layer adjacent to the first and second portions, wherein the layer creates an air gap between the layer, the first and second portions and the IC wafer.

In other features, the IC wafer comprises a silicon wafer. The method further includes encapsulating at least part of the IC wafer, the layer and the first and second portions. The layer comprises at least one of glass and silicon. The method further includes arranging a conductive material adjacent to the first and second portions. The method further includes arranging the air gap between the circuit component, the layer and the first and second portions. The circuit component comprises at least one of an oscillator and an inductor. The method further includes the inductor comprises a spiral inductor. The first and second portions comprise glass frit. The method further includes applying the first and second portions to the silicon wafer using one of a screen printing, dipping and masking. The conductive material comprises one of a conductive epoxy and conductive epoxy paint. The layer has a first width that is less than a second width of the silicon wafer. The method further includes providing bond pads on the IC wafer in an outer region of the silicon wafer.

An integrated circuit (IC) package comprises an IC wafer comprising a circuit and a "C"-shaped layer that is arranged adjacent to the substrate and that creates an air gap between the "C"-shaped layer and the circuit of the IC wafer.

In other features, a molding material that encapsulates at least part of the IC wafer and the "C"-shaped layer. The "C"-shaped layer comprises at least one of glass and silicon. The circuit component comprises at least one of an oscillator and an inductor. The inductor comprises a spiral inductor.

A method for providing an integrated circuit (IC) package comprises providing an IC wafer comprising a circuit and arranging a "C"-shaped layer adjacent to the substrate, wherein the "C"-shaped layer creates an air gap between the "C"-shaped layer and the circuit of the IC wafer.

In other features, the method includes encapsulating at least part of the IC wafer and the "C"-shaped layer. The "C"-shaped layer comprises at least one of glass and silicon. The circuit component comprises at least one of an oscillator and an inductor. The inductor comprises a spiral inductor.

Further areas of applicability of the present invention will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the invention, are intended for purposes of illustration only and are not intended to limit the scope of the invention.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a block diagram showing an aspect of a crystal oscillator emulator.

FIG. **2** is a table showing a relationship between temperature and correction factor.

FIG. **3** is a graph showing a relationship between temperature and correction factor.

FIG. **4** is a block diagram showing an aspect of a crystal oscillator emulator.

FIG. **5** is a two-dimensional view of an aspect of a crystal oscillator emulator connected to external impedances.

FIG. **6** is a detailed block diagram of an aspect of a crystal oscillator emulator connected to an external impedance.

FIGS. **7**A and **7**B are diagrams showing relationships between an external impedance value and a digital value.

FIG. **8** is a block diagram of an aspect of an oscillator assembly for generating an output having a periodic waveform.

FIG. **9** is a block diagram of an aspect of a spread spectrum generator.

FIG. **10** is a flow diagram of an operation for emulating a crystal oscillator.

FIG. **11** is a block diagram of an aspect of a low power oscillator.

FIG. **12** is a block diagram of another aspect of a low power oscillator.

FIG. **13** is a functional block diagram of an integrated circuit including one or more circuits and a crystal oscillator emulator that generates a clock signal for the one or more circuits.

FIG. **14** is a functional block diagram of an integrated circuit including a processor and a crystal oscillator emulator that generates a clock signal for the processor.

FIG. **15** is a functional block diagram of an integrated circuit including a processor and a crystal oscillator emulator that generates a clock signal for the processor and that employs an external component for setting clock speed.

FIG. **16** is a functional block of an integrated circuit including one or more circuits, a crystal oscillator emulator and a clock divider that generates clock signals at one or more other clock frequencies.

FIG. **17** is a functional block of an integrated circuit including a processor, one or more circuits, a crystal oscillator emulator and a clock divider that generates clock signals at other clock frequencies.

FIG. **18** is a functional block of an integrated circuit including a processor, a graphic processor, one or more circuits, memory and a crystal oscillator emulator that generates clock signals.

FIG. **19** is a functional block diagram of an integrated circuit including a processor and the low power oscillator of FIG. **11**.

FIG. **20** is a functional block diagram illustrating an integrated circuit that is encapsulated in a packaging material according to the prior art;

FIG. **21** is a functional block diagram illustrating an integrated circuit with a temperature compensated on-chip semiconductor oscillator that is encapsulated in a packaging material having a low dielectric loss according to the present invention;

FIG. **22** illustrates one exemplary implementation of the integrated circuit package of FIG. **21** in further detail;

FIG. **23** is a side cross-sectional view of an alternate integrated circuit package including an on-chip semiconductor oscillator according to the present invention;

FIG. **24** is a side cross-sectional view of an alternate integrated circuit package including an on-chip semiconductor oscillator according to the present invention;

FIG. **25** is a plan cross-sectional view illustrating the integrated circuit package of FIG. **24** in further detail;

FIG. **26** is a functional block diagram illustrating tuning of a capacitor of an on-chip semiconductor oscillator based upon temperature compensation;

FIG. **27** is a functional block diagram of a fractional phase locked loop (PLL) that includes a temperature compensation input;

FIG. **28** is a functional block diagram of a Delta-Sigma fractional phase locked loop that includes a temperature compensation input;

FIG. **29** is a flow chart illustrating steps for measuring sampling calibration points and using a linear curve fitting algorithm to generate calibration data between the sample calibration points;

FIG. **30** is a flow chart illustrating steps for measuring sampling calibration points and using higher order curve fitting algorithms to generate calibration data between the sample calibration points;

FIG. **31**A is a functional block diagram of a hard disk drive;

FIG. **31**B is a functional block diagram of a digital versatile disk (DVD);

FIG. **31**C is a functional block diagram of a high definition television;

FIG. **31**D is a functional block diagram of a vehicle control system;

FIG. **31**E is a functional block diagram of a cellular phone;

FIG. **31**F is a functional block diagram of a set top box;

FIG. **31**G is a functional block diagram of a media player;

FIG. **32**A is a side cross-sectional view of an alternate integrated circuit package including an annealed glass paste and/or epoxy layer formed on at least part of a silicon wafer;

FIG. **32**B is a side cross-sectional view of an alternate integrated circuit package including an annealed glass paste and/or epoxy layer formed on at least part of a silicon wafer and a conductive material layer formed on at least part of the annealed glass paste and/or epoxy layer;

FIG. **32**C is a side cross-sectional view of an alternate integrated circuit package including spaced annealed glass paste layers formed on selected portions of a silicon wafer;

FIG. **32**D is a side cross-sectional view of an alternate integrated circuit package including spaced annealed glass paste and/or epoxy layers and conductive material layers formed on selected portions of a silicon wafer;

FIG. **33**A is a side cross-sectional view of an alternate integrated circuit package including an annealed glass paste and/or epoxy layer and a conductive material layer adjacent to circuits of a silicon wafer;

FIG. **33**B is a side cross-sectional view of an alternate integrated circuit package including an annealed glass paste

and/or epoxy layer and a conductive material layer adjacent to an oscillator of a silicon wafer;

FIG. **33**C is a side cross-sectional view of an alternate integrated circuit package including an annealed glass paste and/or epoxy layer and a conductive material layer adjacent to an inductor of a silicon wafer;

FIG. **33**D is a side cross-sectional view of an alternate integrated circuit package including an annealed glass paste and/or epoxy layer and a conductive material layer adjacent to an inductor in an oscillator circuit of a silicon wafer;

FIGS. **34**A-**34**D are side cross-sectional views of alternate integrated circuit packages including annealed glass paste and/or epoxy portions and a glass or silicon layer that create an air gap;

FIGS. **35**A-**35**B are side cross-sectional views of alternate integrated circuit packages including a "C"-shaped glass or silicon layer that creates an air gap;

FIGS. **36**A-**36**C are side cross-sectional views of a wafer including multiple integrated circuit packages including annealed glass paste and/or epoxy portions and a glass or silicon layer that create air gaps;

FIGS. **37**A-**37**B are side-cross-sectional views of integrated circuit packages including annealed glass paste and/or epoxy portions that have been coated with a conductive material; and

FIG. **38** illustrates exemplary steps of a method for fabricating the integrated circuit packaging of FIGS. **32**A-**32**D.

Like reference symbols in the various drawings indicate like elements.

DESCRIPTION

FIG. **1** shows an aspect of a crystal oscillator emulator **10** for generating an output signal **12** having a precise frequency. The crystal oscillator emulator **10** may be constructed on a single semiconductor die using any process including a Complementary-Metal-Oxide-Semiconductor (CMOS) process.

The crystal oscillator emulator **10** may include a semiconductor oscillator **14** to generate the output signal **12**. Any type of semiconductor oscillator may be used including LC oscillators, RC oscillators, and ring oscillators. The semiconductor oscillator **12** includes a control input **16** to vary the frequency of the output signal. The control input **16** may be any electrical input that effects a controlled change in the output signal frequency such as the supply voltage of a ring oscillator and a voltage input to a varactor of an LC oscillator.

A non-volatile memory **18** includes calibration information **20** for controlling the output signal frequency as a function of temperature. Any type of non-volatile memory may be employed including content addressable memory (CAM). The calibration information **20** may include a correction factor to be applied to the control input **16** of the semiconductor oscillator **14** to control the output signal frequency. The calibration information **20** may be a function of a change in temperature from a calibration temperature to an operating temperature, as well as being a function of absolute temperature.

A temperature sensor **22** may sense the temperature of the semiconductor die. Preferably, the temperature sensor is located on the semiconductor die in the vicinity of the semiconductor oscillator **14**. Any type of temperature sensor **22** may be used including thermistors and infrared detectors. The temperature sensor **22** may be configured to measure a change in temperature from a baseline temperature or the present temperature.

FIG. **2** shows a storage technique **30** for storing the calibration information **20** in the non-volatile memory **18**. The storage technique **30** may be any form of database including CAM, indexing schemes, look-up tables, and hash tables.

FIG. **3** shows a series of exemplary graphs **32** of correction factor values versus temperature for maintaining a constant output signal frequency for the crystal oscillator emulator **10**. The data for constructing the curve may be attained in any manner including device-level testing and batch-mode testing.

Exemplary device-level testing may include testing each device to determine correction factors to be applied to the semiconductor oscillator to maintain a constant output frequency with changes in temperature. In one scheme, a baseline value for the semiconductor oscillator control input is determined for a predetermined frequency and at a predetermined temperature of the semiconductor die of the device such as the lowest operating temperature. The baseline value may be measured directly or interpolated from measurement of another device characteristic. Baseline values may also be measured for each potential output frequency. Also, baseline values for each potential output frequency may be extrapolated from the baseline value for the predetermined frequency such as by using a known circuit relationship. The baseline values for each potential output frequency may be stored as absolute values or as a ratio, a frequency factor, to compute the baseline values from a single baseline value.

The temperature of the semiconductor die is then increased from about the lowest operating temperature to about the maximum operating temperature in discrete steps. The number of discrete steps is preferably limited to about six temperature levels to reduce testing costs, but any number of discrete steps may be used. Preferably, an on-chip heater is used to heat the semiconductor die, but any means of varying the temperature of the semiconductor die may be employed. At each discrete step, the semiconductor die temperature and the correction factor for maintaining the output at a constant frequency may be measured.

The correction factor is preferably a ratio to be applied to the baseline value to obtain an adjusted value for the control input. The calibration factor may range from any baseline value such as 1. Preferably, a single correction factor is computed for each temperature step, to be applied to the semiconductor oscillator to maintain the output signal at any one of a multitude of predetermined frequencies. For example, if a correction factor of 1.218 is determined to correspond to a change in temperature of 45 C, then the control input of the semiconductor oscillator may be adjusted as a function of the correction factor such as by changing the control input in proportion to the correction factor. In another alternative, the correction factor may be applied to the baseline value corresponding to the desired output frequency to generate a calibrated value to which the control input is adjusted. In another alternative, correction factors may be measured corresponding to each of several output frequencies at each temperature step.

Batch-mode testing of crystal oscillator emulators **10** to obtain calibration information **20** may advantageously decrease costs by reducing the number of measurements for a batch of semiconductor dies. In batch-mode testing, the testing results for a subset of crystal oscillator emulators **10** from the same batch of semiconductor dies may be used for all of the devices in the batch. The subset of crystal oscillator emulators that are tested may range from one to any proportion of the total quantity of devices. For example, a single crystal oscillator emulator **10** may be tested and the resulting batch calibration information stored in each of the devices in the

batch. In addition, each of the crystal oscillator emulators **10** may be tested for a subset of calibration information such as the output frequency at a baseline temperature. The subset of device specific calibration information may be used to modify the batch calibration information stored in each device.

FIG. **4** shows another aspect of a crystal oscillator emulator **40**. The crystal oscillator emulator **40** is similar to crystal oscillator **10** in function with similar corresponding elements numbered in the range of **40-52**, except that crystal oscillator emulator **40** may also include one or more of a heater **54**, a controller **56**, and a select input **58** alone or in combination.

The heater **54** may be located on the semiconductor die in the vicinity of the semiconductor oscillator **44** to provide a source of local heating. Any type of heater **54** may be used including transistor heaters and resistive heaters. The heater **54** may be operated in response to an input from the temperature sensor **52** to control the temperature of the semiconductor die. The heater **54** may increase the semiconductor die temperature to a level that corresponds to one of the temperature levels for which correction factors have been determined. In addition, a package having a high thermal impedance may enclose the crystal oscillator emulator **40**.

In one case, the heater **54** may increase the semiconductor die temperature to the maximum operating temperature. Here, during device or batch level testing only the correction factor corresponding to the maximum operating temperature would have to be determined, leading to reduced costs.

The heater **54** may also be controlled to raise the semiconductor die temperature to one of several predetermined temperature levels for which correction factors have been determined. A second temperature sensor may sense an external temperature such as an ambient temperature or an assembly temperature. The heater **54** then may increase the semiconductor die temperature to the nearest of the predetermined temperature levels while continuously changing the control input during the temperature transition using extrapolated values computed from the correction factors.

The controller **56** may add extra functionality by for example controlling the heater **54** in response to multiple temperature sensors or manipulating the calibration information **50** to derive values for the control input that correspond to intermediate temperatures. The controller **56** may be any type of entity including a processor, logic circuitry, and a software module.

The select input **58** may be used for selecting specific output frequencies from within a range of output frequencies. The output frequency may be selected as a function of the impedance of an external component connected to the select input. The external component may be used directly as a portion of the semiconductor oscillator to select the output frequency, or indirectly such as selecting values of impedance within a predetermined range may correspond to predetermined output frequencies. The external component may be any component, but is preferably a passive component such as a resistor or capacitor.

FIG. **5** shows an aspect of a crystal oscillator emulator **100** having, for example, two select pins **102** and **104** to connect to two external impedances **106** and **108**. One or more pins may be used to interface to the external component(s). The crystal oscillator emulator **100** probes or derives information from the external components connected to the select pins **102** and **104**. The derived information may have three or more predetermined level ranges that correspond to selected levels of the emulator characteristics. For example, a single pin connected to an external resistor may be used to select any one of 16 output frequency levels. The resistance of the external resistor is preferably selected to be one of 16 predetermined standard values. Each of the 16 values of resistance corresponds to one of the 16 output frequency levels. In addition, low precision passive components are preferably used as the external components to reduce cost and inventory. Each external component may have multiple, N, predetermined nominal values that each correspond to the selection of a predetermined characteristic level. If one pin is used, then N different characteristic levels may be selected. If two pins are used, then N*N different characteristic levels may be selected, and so forth for an increasing number of selection pins. The types of device characteristics that for example may be selected include output frequency, frequency tolerance, and baseline correction factor. For example, the crystal oscillator emulator **100** may have a single select pin **102** connected to an external resistor that may have a nominal value selected from a group of 16 predetermined values. Each of the 16 predetermined values has a measured value range which corresponds to one of 16 predetermined output frequency levels possibly ranging from 1 MHz to 100 MHz.

The external impedances **106** and **108** are preferably resistors, capacitors, or combinations of resistors and capacitors, but may be any component that exhibits predominantly an inductance, resistance, capacitance, or combination thereof. The external impedances **106** and **108** may be connected directly or indirectly from any energy source such as Vdd and ground or any suitable reference to the pins **102** and **104**. For example, the external impedance **106** may be connected through a resistor/transistor network to Vdd and through a capacitor network to the select pin **102**.

The crystal oscillator emulator **100** may determine a predetermined select value corresponding to the measured value of the impedance connected to a select pin. Preferably, the impedance is selected to have a standard value such as nominal resistance values corresponding to resistors having a 10% tolerance (e.g. 470, 560, 680, . . .) to reduce device and inventory costs. To account for measurement tolerances and the tolerance of the external impedance, a range of impedance values may correspond to a single select value. The select value is preferably a digital value, but may also be an analog value. For example, values of measured resistance from 2400 ohms to 3000 ohms may be associated with a digital value corresponding to 2. While values of measured resistance from 3001 ohms to 4700 ohms are associated with a digital value corresponding to 3. The measured resistance includes variations due to tolerances of the external impedance and the internal measurement circuit. The impedance measured at each select pin is used to determine a corresponding digital value. The range of digital values may include 3 or more digital values and preferably range from 10 to 16 digital values per select pin. The digital values corresponding to each select pin may be used in combination to describe memory addresses. For example, a device having three select pins each to interface to impedance values that are mapped into one of 10 digital values, may describe 1000 memory addresses or lookup table values. The contents of the storage locations corresponding to the memory addresses are used to set a value for an output or internal characteristic of the device. Another exemplary device may include two select pins, each configured to interface to external impedances that are mapped to a digital value within a range of 10 values. The digital values in combination may describe 100 memory addresses or lookup table values that may each contain data for setting a characteristic of the crystal oscillator emulator **100**.

FIG. **6** shows a block diagram of an aspect of a crystal oscillator emulator **120**. The crystal oscillator emulator **120** includes a select pin **122** to interface to an external impedance **124** that is used for selecting a configuration of the crystal

oscillator emulator **120**. The external impedance **124** is similar in function and scope to the external impedances **116** and **118**.

A measurement circuit **126** connected to the select pin **122** measures an electrical characteristic that is a function of the external impedance **124**. For example, a current, may be supplied to the external impedance and the voltage that is developed across the external impedance **124** then measured. Also, a voltage may be impressed across the external impedance **124** and then measure the current. Any measurement technique for measuring passive components may be used to measure the electrical characteristic including dynamic as well as static techniques. Exemplary measurement techniques include timing circuits, analog to digital converters (ADCs), and digital to analog converters (DACs). Preferably, the measurement circuit has a high dynamic range. The measurement circuit **126** may generate an output having a value corresponding to the value of the external impedance **124**. The output may be either digital or analog. The same output value preferably represents a range of external impedance values to compensate for value variations such as tolerances in the external impedance value, interconnect losses, and measurement circuit tolerances due to factors including process, temperature, and power. For example, all measured external impedance values ranging from greater than 22 up to 32 ohms may correlate to a digital output value of "0100". While measured external impedance values ranging from greater than 32 up to 54 ohms may correlate to a digital output value of "0101". The actual external impedance values are a subset of the measured external impedance value to account for the value variations. For example, in the above cases the actual external impedance values might be from 24 to 30 ohms and from 36 to 50 ohms. In each case an inexpensive low precision resistor may be selected to have a value centered within the range, such as 27 ohms and 43 ohms. In this way, inexpensive low precision components may be used to select amongst a range of high precision outputs. The select value may be used directly as a variable value to control a device characteristic of the crystal oscillator emulator **120**. The variable value may also be determined indirectly from the select value.

A storage circuit **127** may include variable values that may be selected as a function of the select value. The storage circuit **127** may be any type of storage structure including content addressable memory, static and dynamic memory, and look-up tables.

For the case that the measurement circuit **126** generates output values that have a one-to-one correspondence to the external impedance values, a digital value determiner **128** may then set the output value to a select value that corresponds to a range of external impedance values.

FIG. **7**A shows a relationship between groups of impedance values **150** and associated select values **154**. The groups of impedance values **150** may have a one-to-one correspondence to groups of digital output values **152** which are converted to the select values **154** associated with each of the groups of impedance values **150**. The impedance values ranging from a minimum impedance value to a maximum impedance are separated in into three or more groups, with each group having a nominal impedance. The nominal impedance values of each of the groups may be selected to have a spacing between nominal impedance values. Here, the nominal values, 27 ohms and 43 ohms, of the groups of impedance values have a spacing of 16 ohms. The spacing between the groups of impedance values is preferably based on geometric progression, however any mathematical relationship may be used to establish spacing between the groups such as logarithmic, linear, and exponential. The spacing between impedance groups may be based on any impedance value of the groups including a nominal value, an average value, a mean value, a starting value, and an ending value. Factors that influence selection of the impedance range of the groups and the spacing may include various tolerances such as the tolerance of the external impedance, the tolerance of internal voltage and current sources, and the tolerance of the measurement circuit. The tolerances may for example be caused by process, temperature, and power variations.

FIG. **7**B shows a relationship between ranges of impedance values **156** and associated select values **158**. The ranges of impedance values **156** have a direct correspondence to the select values **158**. The impedance values ranging from a minimum impedance value to a maximum impedance are separated in into three or more groups, with each group having a nominal impedance. The nominal impedance values of each of the groups may be selected to have a spacing between nominal impedance values. Here, the nominal values, 27 ohms and 43 ohms, of the groups of impedance values have a spacing of 16 ohms. This direct correspondence between the ranges of impedance values **156** and associated select values **158** may be implemented by, for example, a nonlinear analog to digital converter (not shown).

Referring back to FIG. **6**, an address generator **130** may determine memory locations corresponding to the digital output values associated with external impedances connected to the select pins. The memory locations may be grouped in any manner such as a list for a single select pin, a lookup table for two select pins, and a third order table for three select pins.

A controller **132** may set a device characteristic of the crystal oscillator emulator **120** as a function of the variable value. The variable value may be generated directly by the measurement circuit, determined indirectly from the select value, and determined from the contents of a memory location corresponding to the external impedance values connected to the select pins.

The select pin **124** may also be used for implementing an additional function such as power down (PD), power enable, mode selection, reset, and synchronous operation. In this aspect, the select pin **124** becomes a multi-purpose select pin **124** for configuring the crystal oscillator emulator **120** as well as implementing the additional function.

In one aspect, a first range of impedance values connected to the multi-purpose select pin **124** may be used to configure the crystal oscillator emulator **120**, while operation of the additional function may be controlled by a voltage or current impressed on the multi-purpose select pin **124**, or impedance values outside the first range of impedance values.

FIG. **8** shows an aspect of an oscillator assembly **200** to generate an output having a periodic waveform. The oscillator assembly **200** includes a crystal oscillator emulator **202** to drive a phase lock loop (PLL) **204**. The crystal oscillator emulator **202** may be similar in function and structure to the aspects of the crystal oscillator emulators described above. The oscillator assembly **200** may include any type of PLL **204** such as digital PLLs and analog PLLs.

Multi-purpose select pins **206** and **208** may be used for selection of the operating parameters for the PLL **204** such as the divider factor. The multi-purpose select pins **206** and **208** may also be used for control and operation of the crystal oscillator emulator **202** such as output frequency selection and reception of a reference clock for calibration. External resistors **210** and **212** may be connected to the multi-purpose select pins **206** and **208** to select the operating frequency. The ranges of values of the external resistors **210** and **212** correspond to the selection of different operating frequencies.

Each external resistor **210** and **212** may be used to select one of 16 predetermined operating frequencies. In combination, the external resistors **210** and **212** may select from amongst 256 operating frequencies. To control multiple functions, each of the multi-purpose select pins **206** and **208** may receive signals within different voltage ranges. For example, one multi-purpose select pin **206** may connect to an external resistor **210** across which a voltage in the range of 0 to 2 volts may be developed to determine the resistance, and the multi-purpose select pin **206** may also receive a reference clock signal operating in a range of 2 to 3 volts. A decoder **214** may detect signals on the multi-purpose select pins **206** and **208**.

FIG. **9** shows a spread spectrum oscillator **300** for generating an output signal having a variable frequency. The spread spectrum oscillator **300** includes a crystal oscillator emulator **302** connected to a PLL **304**. A frequency control device connected to the crystal oscillator emulator **302** may dynamically control the output frequency of the crystal oscillator emulator **302**. The frequency control device may be any device or technique including a varactor, controlling the bias current source of the semiconductor oscillator, and controlling the control input voltage applied to the resonant capacitors of the semiconductor oscillator.

FIG. **10** shows the operation of an aspect of a crystal oscillator emulator. At block **400**, a semiconductor oscillator is provided for generating an output signal having a periodic waveform. Continuing to block **402**, the semiconductor oscillator may be calibrated to generate a constant frequency over a predetermined range of temperature. In one aspect, the calibration may include varying the temperature of the semiconductor die over a predetermined temperature range and measuring calibration information for maintaining a constant output frequency. The die temperature may be measured in the vicinity of the semiconductor oscillator. The calibration information may include control input values versus die temperatures for maintaining a constant output frequency. The calibration information may be stored in non-volatile memory on the semiconductor die. At block **404**, an operating frequency may be determined by probing an external component. Continuing to block **406**, the semiconductor oscillator generates an output signal having an operating frequency. At block **408**, the temperature of the semiconductor die is determined in the vicinity of the semiconductor oscillator. Continuing to block **410**, the semiconductor die may be heated or cooled to control the die temperature to one or more predetermined temperature levels. At block **412**, the control input may be controlled as a function of the die temperature to compensate for changes in the operating frequency of the output signal caused by temperature changes. The stored calibration information may be used to control the control input. The calibration information may be used directly for die temperatures that correspond to stored temperatures. For other die temperatures, the control input value may be extrapolated from the stored calibration information. Continuing to block **414**, the frequency of the output signal may be dynamically varied as a function of a frequency control signal.

FIG. **11** shows an aspect of a low power oscillator **320** for generating a periodic signal. The low power oscillator **320** includes a crystal oscillator emulator **322** to calibrate an active silicon oscillator **324**. The crystal oscillator emulator **322** is normally in the off state to reduce power consumption. At predetermined intervals, the crystal oscillator emulator **322** is switched to the powered on state to calibrate the active silicon oscillator **324**. The active silicon oscillator **324** consumes less power than the crystal oscillator emulator **322**, so operating the active silicon oscillator **324** continuously while only operating the crystal oscillator emulator **322** intermittently reduces the overall power consumption of the low power oscillator **320**. Any type of active silicon oscillator may be used including ring oscillators and RC oscillators. The crystal oscillator emulator **324** may be configured in accordance with any of the aspects of the invention as described and shown in this specification.

A summer **326** may determine the frequency error between the active silicon oscillator output and the crystal oscillator emulator output. A controller **328** may generate a control signal, based on the frequency error, to control the frequency of the active silicon oscillator **324**. The controller **328** may also receive temperature information from the crystal oscillator emulator **322**. The temperature information may include temperatures such as the temperature of the semiconductor and the ambient temperature. The controller **328** may include calibration information for the active silicon oscillator **324** similar to the calibration information for the crystal oscillator emulator **322**. The frequency error may be used to set an initial value for the control signal and then the temperature information in combination with the active silicon oscillator calibration information may be used to update the control signal while the crystal oscillator emulator **322** is powered down. In one aspect, the temperature sensing circuit of the crystal oscillator emulator **322** may remain continuously powered so that continuous temperature information may be supplied to the controller **328**. The control signal **334** may be either digital or analog. If the control signal is digital, a digital-to-analog converter (DAC) **330** may convert the control signal to analog.

A regulator **332** may, in response to the control signal **334**, control the supply of power for the active silicon oscillator **324** to adjust the operating frequency. The supply of voltage and/or current to the active silicon oscillator **324** may be controlled. For example, the regulator **332** may control the voltage level of the supply voltage.

In operation, the active silicon oscillator **324** is normally in the on state generating a periodic output signal. The crystal oscillator emulator **322** is normally in the off state. In the off state, either all or a portion of the crystal oscillator emulator **322** may be powered off to conserve power. At a predetermined time, power is applied to the crystal oscillator emulator **322**. The semiconductor oscillator of the crystal oscillator emulator **322** is then calibrated with the stored calibration information. The frequency of the output signal of the crystal oscillator emulator **322** is compared with the frequency of the output signal of the active silicon oscillator **324** to determine the frequency error of the active silicon oscillator **324**. The control signal **334** changes in response to the frequency error, causing a shift in the supply voltage from the voltage regulator **332**, leading to a change in the output frequency of the active silicon oscillator **324**, reducing the frequency error.

FIG. **12** shows an aspect of another low power oscillator **350** for generating a periodic signal. The low power oscillator **350** includes a crystal oscillator emulator **352** in communication with a charge pump oscillator **354**. The crystal oscillator emulator **352** is normally in the powered down state to reduce power consumption. During the powered down state, either all or a portion of the crystal oscillator emulator **352** may be powered down. At predetermined intervals, the crystal oscillator emulator **352** may be powered up and used to calibrate the charge pump oscillator **354**. The predetermined intervals may be determined as a function of any circuit parameter such as operating time, temperature change of the semiconductor, ambient temperature change, temperature of the semiconductor, and supply voltage change.

The charge pump oscillator **354** may include a charge pump **356**, loop filter **358**, voltage controlled oscillator (VCO) **360**, and phase detector **362**. The charge pump oscillator **354** is similar in operation to conventional charge pump oscillators, except that the reference input of the phase detector **362** receives a reference clock signal from the crystal oscillator emulator **352**.

A multiplexer **364** receives the output signals from the crystal oscillator emulator **352** and the charge pump oscillator **354**. One of the output signals is selected and passed through the multiplexer **375** to a phase locked loop **366**. The phase locked loop **366** generates an output signal as a function of the output signals from the crystal oscillator emulator **352** and the charge pump oscillator **354**.

In operation, the charge pump oscillator **354** is normally in the on state generating a periodic output signal. The crystal oscillator emulator **352** is normally in the off state. In the off state, either all or a portion of the crystal oscillator emulator **352** may be powered off to reduce power consumption. At a predetermined time, power is applied to the crystal oscillator emulator **352**. The semiconductor oscillator of the crystal oscillator emulator **352** is then calibrated with the stored calibration information. The output signal of the crystal oscillator emulator **352** is compared with the output signal of the charge pump oscillator **354** to determine the phase error of the charge pump oscillator **324**. The VCO **360** is then controlled to reduce the phase error so that the output signal of the charge pump oscillator **354** is calibrated to the output signal of the crystal oscillator emulator **352**. One of the output signals may then be selected and applied to the PLL **366**.

Referring now to FIGS. **13-15**, an integrated circuit **500** includes a crystal oscillator emulator **502** that generates a clock signal. One or more circuits **504** in the integrated circuit **500** receive the clock signals. The crystal oscillator emulator **502** can be implemented as described above in conjunction with FIGS. **1-12**. The circuits **502** can include a processor **512** as shown in FIG. **14** or other circuits. An external component **506** can optionally be used to select the clock frequency of the crystal oscillator emulator **502** as shown in FIGS. **13** and **15**.

Referring now to FIGS. **16-18**, an integrated circuit **518** includes a clock divider **520** that generates clock signals at other one or more other clock frequencies for circuits **522-1**, **522-2**, . . . , and **522**-N (collectively circuits **522**). The circuits **522** may be interconnected to each other in any manner. The clock divider **520** divides the clock by an integer such as X and/or multiplies the clock signal by Y for 1/X, Y and/or Y/X adjustments. The clock divider **520** may also use one or more additional ratios and/or divisors for producing different clock signals for other circuits **522**. The clock divider **520** outputs N−1 clock signals as shown to N−1 circuits **522** in the integrated circuit **518**.

In FIG. **17**, one of the circuits includes a processor **530**. The processor **530** can be connected to the clock divider **520** instead of and/or in addition to the crystal oscillator emulator **502**. Additional circuits **532-1**, **532-1**, and **532**-N communicate with the clock divider **520**.

In FIG. **18**, the crystal oscillator emulator **502** provides clock signals for a processor **530**, a graphics processor **540**, memory **542** and/or one or more circuits **544** in the integrated circuit **518**. A clock divider (not shown) may also be provided. The processor **530**, graphics processor **540**, memory **542** and/or other circuits **544** may be interconnected in any suitable manner.

Referring now to FIG. **19**, an integrated circuit **600** includes one or more circuits **602-1**, **602-2**, . . . , and **602**-N (collectively circuits **602**) and the low power oscillator **320**, which operates as described above in conjunction with FIG. **11**. One of the circuits may include a processor as shown at **610**. A clock divider (not shown) may also be provided as described above.

Integrated circuits (IC) are typically encased in a packaging material. The packaging material may include plastic. The IC substrate may include pads that are connected to leads of a lead frame by bondwires. The IC substrate, the bondwires and portions of the leads may be encased in the plastic. The properties of the packaging material that is normally used in packaging the IC may change over time. The changes may cause an oscillation frequency of an on-chip oscillator to drift over time. The changes in the packaging may be due to changes in the dielectric loss of the packaging material over time. The changes in the packaging may also be due to water absorption of the packaging material at different humidity levels. As a result, the packaging material may limit the achievable calibrated accuracy.

Referring now to FIG. **20**, an integrated circuit **700** is encapsulated in a packaging material **704** according to the prior art. As can be appreciated, characteristics of the packaging material **704** may change over time and/or as a function of environmental conditions. For example, when the packaging material **704** includes plastic material, the dielectric loss of the plastic material may change over time, which may have an adverse impact upon calibration accuracy. As used herein, the term dielectric loss refers to loss of energy that eventually produces a rise in temperature of a dielectric placed in an alternating electrical field. Heating is due to "molecular friction" of dipoles within the material as the dipoles try to reorient themselves with the oscillating (electrical) field of the incident wave. For example, when heating food in a microwave, the dipoles associated with water in the food vibrate and are heated. Some materials such as certain plastics are not suitable for use in microwaves since they absorb too much heat. These materials have high dielectric loss characteristics. Other materials such as other types of plastics experience little or no heating. These materials have lower dielectric loss characteristics. Since the circuits described herein may operate at microwave frequencies, low dielectric loss materials are preferred.

Water absorption of the plastic material over time may also adversely impact calibration accuracy. Since water has a high dielectric loss, increased water content in the packaging material tends to increase the dielectric loss of the packaging material. In other features, the packaging material may also be a low stress material. High stress materials tend to warp, which may affect circuit characteristics of adjacent circuits such as by changing channel lengths. As used herein, the term low stress refers to packaging materials that tend to be stable and not change the electrical characteristics of the integrated circuit due to changes in stress. In some implementations, the packaging material has a dielectric loss factor (DLF) that is less than or equal to Teflon at the relevant frequency of operation, such as greater than 1 GHz.

Referring now to FIG. **21**, an integrated circuit **710** with an on-chip semiconductor oscillator **711** with temperature compensation is shown encapsulated in a packaging material **714** having a low dielectric loss according to the present invention. The packaging material **714** may be a plastic packaging material having low dielectric loss. As used herein, the term "low dielectric loss" refers to materials having a dielectric loss that is less than or equal to Teflon at a relevant operating frequency of the IC. The operating frequency of the IC may be above 1 GHz and/or 2.4 GHz. The packaging material **714** may also comprise Teflon®, Teflon® PolyChloroTriFluoroEthylene (PCTFE), Teflon® Teflon® fluorinated ethylene propylene copolymer (FEP), perfluoroalkoxy) (PFA), Tef-

zel® and Teflon® copolymer of ethylene and tetrafluoroethylene (ETFE), low dielectric loss plastic, high quality glass, air and/or other materials. Any other packaging materials having dielectric loss that is less than or equal to Teflon are contemplated. The packaging material also may have relatively low water absorption.

Referring now to FIG. **22**, an exemplary implementation of the integrated circuit package of FIG. **21** is shown in further detail. An integrated circuit package **718** includes an integrated circuit **724** that includes pads **728**. Leads **732** of a lead frame **733** are connected by bondwires **734** to the pads **728** of the integrated circuit. As can be appreciated, the integrated circuit includes an on-chip semiconductor oscillator with temperature compensation as described above. Portions of the leads **732**, the bond wires **734** and the integrated circuit **724** are encapsulated in a packaging material **736**. The packaging material **736** may be a plastic packaging material having low dielectric loss. As can be appreciated, other types of packaging such as ball grid array (BGA), flip chip and/or any other suitable packaging technique may be employed in this embodiment and/or others that precede or follow.

Referring now to FIG. **23**, an alternate integrated circuit package **738** includes an on-chip, temperature-compensated semiconductor oscillator **741** according to the present invention. In this embodiment, the semiconductor oscillator **741** comprises an integrated circuit inductor **742**. A glass layer **744** is bonded to the integrated circuit substrate **740** using a very thin epoxy layer **750**. The epoxy layer **750** may have a low dielectric loss. The glass layer **744**, the epoxy layer **750** and the integrated circuit substrate **740** are encapsulated in a packaging material **760**. In this case, the dielectric loss of the packaging material is less critical due to the distance between the inductor **742** and the packaging material **760**. Therefore, changes in the dielectric loss and/or other characteristics of the packaging material **760** are less critical as a function of time. However, the packaging material can be low dielectric loss material. While the glass layer is shown over the entire integrated circuit, the glass layer may be limited to a smaller region immediately adjacent to the semiconductor oscillator.

Referring now to FIGS. **24** and **25**, an alternate integrated circuit package including an on-chip semiconductor oscillator according to the present invention is shown. This embodiment is similar to that shown and described above in conjunction with FIG. **23**. However, the glass layer **744** defines a cavity **746**. The cavity **746** is adjacent to, aligned with and extends over the inductor **742**. An air cavity **752** is formed between the inductor **742** and the glass layer **744**. A thin epoxy layer **750** is formed between the glass layer **744** and the integrated circuit substrate **740** in areas other than the cavity **746**. The glass layer **744** may be etched to define the cavity and dipped in epoxy. Adjacently, the glass layer may include multiple layers of glass and at least one layer has a cavity formed therein.

Referring now to FIG. **26**, a capacitor of an on-chip semiconductor oscillator may be adjusted based upon temperature compensation as previously described above. As can be appreciated, however, there are other ways of adjusting the oscillating frequency independent from adjusting the capacitor and/or inductor of the semiconductor oscillator.

Referring now to FIG. **27**, an integrated circuit **830** includes a fractional phase locked loop **831** with a temperature compensation input. The fractional phase locked loop **831** includes a phase frequency detector **836** that receives an output of the integrated circuit oscillator **832**, which operates as described above. The phase frequency detector **836** generates a differential signal based on a difference between a reference frequency and a VCO frequency. The differential signal is output to a charge pump **840**. An output of the charge pump **840** is input to an optional loop filter **844**. An output of the loop filter **844** is input to a voltage controlled oscillator (VCO), which generates a VCO output having a frequency that is related to a voltage input thereto. An output of the VCO **846** is fed back to a scaling circuit **850**. The scaling circuit **850** selectively divides the VCO frequency by N or N+1. While N and N+1 divisors are employed, the divisors may have other values.

An output of the scaling circuit **850** is fed back to the phase frequency detector **836**. A temperature sensor **850** measures a temperature of the integrated circuit **830** in the region near the IC oscillator **832**. The temperature sensor **850** outputs a temperature signal that is used to address calibration information **858** that is stored in memory **856**. The selected calibration information is used to adjust the scaling circuit **850**. The selected calibration information adjusts a ratio of the divisors N and N+1 that are used by the scaling circuit **844**.

Referring now to FIG. **28**, a Delta-Sigma fractional phase locked loop **858** is shown for an integrated circuit **860** that includes a temperature compensation input. The selected calibration information is used to adjust an output of a Sigma Delta modulator **870**. The selected calibration information may adjust a modulation between the divisors N and N+1 that are used by the scaling circuit **844**.

Referring now to FIG. **29**, a flow chart **900** illustrates steps for measuring sampling calibration points using a linear curve fitting algorithm to generate the calibration data. Control begins with step **902**. In step **904**, control measures sample calibration points at a plurality of temperatures. In step **906**, linear curve fitting algorithms are used to generate curves for other temperature points between the sample points. In step **908**, control ends.

Referring now to FIG. **30**, a flow chart **920** illustrating steps for measuring sampling calibration points and using higher order curve fitting algorithms to generate the calibration data. The steps shown in FIG. **29** may be implemented using a computer that includes a processor and memory. Control begins with step **902**. In step **924**, control measures sample calibration points at a plurality of temperatures. In step **926**, higher order curve fitting algorithms are used to generate curves for other temperature points between the sample points. In step **928**, control ends.

Referring now to FIGS. **31**A-**31**G, various exemplary implementations of the present invention are shown. Referring now to FIG. **31**A, the present invention can be implemented in a hard disk drive **1000**. The present invention may implement any integrated circuit such as either or both signal processing and/or control circuits, which are generally identified in FIG. **31**A at **1002**. In some implementations, the signal processing and/or control circuit **1002** and/or other circuits (not shown) in the HDD **1000** may process data, perform coding and/or encryption, perform calculations, and/or format data that is output to and/or received from a magnetic storage medium **1006**.

The HDD **1000** may communicate with a host device (not shown) such as a computer, mobile computing devices such as personal digital assistants, cellular phones, media or MP3 players and the like, and/or other devices via one or more wired or wireless communication links **1008**. The HDD **1000** may be connected to memory **1009** such as random access memory (RAM), low latency nonvolatile memory such as flash memory, read only memory (ROM) and/or other suitable electronic data storage.

Referring now to FIG. **31**B, the present invention can be implemented in a digital versatile disc (DVD) drive **1010**. The present invention may implement any integrated circuit such

as either or both signal processing and/or control circuits, which are generally identified in FIG. **31**B at **1012**, and/or mass data storage of the DVD drive **1010**. The signal processing and/or control circuit **1012** and/or other circuits (not shown) in the DVD **1010** may process data, perform coding and/or encryption, perform calculations, and/or format data that is read from and/or data written to an optical storage medium **1016**. In some implementations, the signal processing and/or control circuit **1012** and/or other circuits (not shown) in the DVD **1010** can also perform other functions such as encoding and/or decoding and/or any other signal processing functions associated with a DVD drive.

The DVD drive **1010** may communicate with an output device (not shown) such as a computer, television or other device via one or more wired or wireless communication links **1017**. The DVD **1010** may communicate with mass data storage **1018** that stores data in a nonvolatile manner. The mass data storage **1018** may include a hard disk drive (HDD). The HDD may have the configuration shown in FIG. **31**A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The DVD **1010** may be connected to memory **1019** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage.

Referring now to FIG. **31**C, the present invention can be implemented in a high definition television (HDTV) **1020**. The present invention may implement any integrated circuit such as either or both signal processing and/or control circuits, which are generally identified in FIG. **31**E at **1022**, a WLAN interface and/or mass data storage of the HDTV **1020**. The HDTV **1020** receives HDTV input signals in either a wired or wireless format and generates HDTV output signals for a display **1026**. In some implementations, signal processing circuit and/or control circuit **1022** and/or other circuits (not shown) of the HDTV **1020** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other type of HDTV processing that may be required.

The HDTV **1020** may communicate with mass data storage **1027** that stores data in a nonvolatile manner such as optical and/or magnetic storage devices. At least one HDD may have the configuration shown in FIG. **31**A and/or at least one DVD may have the configuration shown in FIG. **31**B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The HDTV **1020** may be connected to memory **1028** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The HDTV **1020** also may support connections with a WLAN via a WLAN network interface **1029**.

Referring now to FIG. **31**D, the present invention implements any integrated circuit in a control system of a vehicle **1030**, a WLAN interface and/or mass data storage of the vehicle control system. In some implementations, the present invention implement a powertrain control system **1032** that receives inputs from one or more sensors such as temperature sensors, pressure sensors, rotational sensors, airflow sensors and/or any other suitable sensors and/or that generates one or more output control signals such as engine operating parameters, transmission operating parameters, and/or other control signals.

The present invention may also be implemented in other control systems **1040** of the vehicle **1030**. The control system **1040** may likewise receive signals from input sensors **1042** and/or output control signals to one or more output devices **1044**. In some implementations, the control system **1040** may be part of an anti-lock braking system (ABS), a navigation system, a telematics system, a vehicle telematics system, a lane departure system, an adaptive cruise control system, a vehicle entertainment system such as a stereo, DVD, compact disc and the like. Still other implementations are contemplated.

The powertrain control system **1032** may communicate with mass data storage **1046** that stores data in a nonvolatile manner. The mass data storage **1046** may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in FIG. **31**A and/or at least one DVD may have the configuration shown in FIG. **31**B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The powertrain control system **1032** may be connected to memory **1047** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The powertrain control system **1032** also may support connections with a WLAN via a WLAN network interface **1048**. The control system **1040** may also include mass data storage, memory and/or a WLAN interface (all not shown).

Referring now to FIG. **31**E, the present invention can be implemented in a cellular phone **1050** that may include a cellular antenna **1051**. The present invention may implement any integrated circuit such as either or both signal processing and/or control circuits, which are generally identified in FIG. **31**E at **1052**, a WLAN interface and/or mass data storage of the cellular phone **1050**. In some implementations, the cellular phone **1050** includes a microphone **1056**, an audio output **1058** such as a speaker and/or audio output jack, a display **1060** and/or an input device **1062** such as a keypad, pointing device, voice actuation and/or other input device. The signal processing and/or control circuits **1052** and/or other circuits (not shown) in the cellular phone **1050** may process data, perform coding and/or encryption, perform calculations, format data and/or perform other cellular phone functions.

The cellular phone **1050** may communicate with mass data storage **1064** that stores data in a nonvolatile manner such as optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in FIG. **31**A and/or at least one DVD may have the configuration shown in FIG. **31**B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The cellular phone **1050** may be connected to memory **1066** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The cellular phone **1050** also may support connections with a WLAN via a WLAN network interface **1068**.

Referring now to FIG. **31**F, the present invention can be implemented in a set top box **1080**. The present invention may implement any integrated circuit such as either or both signal processing and/or control circuits, which are generally identified in FIG. **31**F at **1084**, a WLAN interface and/or mass data storage of the set top box **1080**. The set top box **1080** receives signals from a source such as a broadband source and outputs standard and/or high definition audio/video signals suitable for a display **1088** such as a television and/or monitor and/or other video and/or audio output devices. The signal processing and/or control circuits **1084** and/or other circuits (not shown) of the set top box **1080** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other set top box function.

The set top box **1080** may communicate with mass data storage **1090** that stores data in a nonvolatile manner. The mass data storage **1090** may include optical and/or magnetic storage devices for example hard disk drives HDD and/or

DVDs. At least one HDD may have the configuration shown in FIG. **31**A and/or at least one DVD may have the configuration shown in FIG. **31**B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The set top box **1080** may be connected to memory **1094** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The set top box **1080** also may support connections with a WLAN via a WLAN network interface **1096**.

Referring now to FIG. **31**G, the present invention can be implemented in a media player **1100**. The present invention may implement any integrated circuit such as either or both signal processing and/or control circuits, which are generally identified in FIG. **31**G at **1104**, a WLAN interface and/or mass data storage of the media player **1100**. In some implementations, the media player **1100** includes a display **1107** and/or a user input **1108** such as a keypad, touchpad and the like. In some implementations, the media player **1100** may employ a graphical user interface (GUI) that typically employs menus, drop down menus, icons and/or a point-and-click interface via the display **1107** and/or user input **1108**. The media player **1100** further includes an audio output **1109** such as a speaker and/or audio output jack. The signal processing and/or control circuits **1104** and/or other circuits (not shown) of the media player **1100** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other media player function.

The media player **1100** may communicate with mass data storage **1110** that stores data such as compressed audio and/or video content in a nonvolatile manner. In some implementations, the compressed audio files include files that are compliant with MP3 format or other suitable compressed audio and/or video formats. The mass data storage may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in FIG. **31**A and/or at least one DVD may have the configuration shown in FIG. **31**B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The media player **1100** may be connected to memory **1114** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The media player **1100** also may support connections with a WLAN via a WLAN network interface **1116**. Still other implementations in addition to those described above are contemplated.

Referring now to FIGS. **32**A-**32**D, an integrated circuit package is shown that incorporates an annealed glass paste or epoxy as a layer and/or "islands" adjacent to one or more selected features of a silicon wafer. One or more "islands" of the annealed glass paste or epoxy layer can be made on portions of one or both sides of the silicon wafer. In FIG. **32**A, an alternate integrated circuit package **1200** includes a silicon wafer **1204**. An annealed glass paste layer or portions **1206** is/are formed on the silicon wafer **1204**. A molding material **1208** may be used to encapsulate all or part of the silicon wafer **1204**. The annealed glass paste layer **1206** also reduces the change in stress over time. The annealed glass paste layer **1206** tends to isolate all or part of the silicon wafer **1204** from variations in the dielectric properties such as dielectric loss of the molding material **1208**.

The silicon wafer **1204** may include a semiconductor oscillator as described above. The annealed glass paste layer **1206** may include a glass paste having a relatively low annealing temperature. The low annealing temperature may be lower than a temperature that would damage the silicon wafer **1204**. The glass paste layer **1206** may include glass frit paste. The glass paste layer may be applied in any suitable manner. The glass paste layer may be applied using a screen printing approach, a dipping approach, a masking approach, and/or using any other suitable approach.

In FIG. **32**B, an alternate integrated circuit package **1210** includes a conductive material layer or coating **1212** that is applied to the glass paste or epoxy layer **1204**. The conductive material layer **1212** may include a layer of conductive epoxy. The conductive material layer **1212** may be applied as a liquid and cured. The conductive material layer **1212** may include conductive epoxy paint. The conductive material layer **1212** may be applied in any suitable fashion including dipping the silicon wafer **1204** into a container such as a dish that contains the conductive material. The conductive material layer **1212** tends to reduce electro-magnetic interference from external devices.

In FIG. **32**C, an integrated circuit package **1220** includes the annealed glass paste layer **1206**, which is applied to selected portions of the silicon wafer **1204**. In FIG. **32**D, an integrated circuit package **1230** includes the annealed glass paste or epoxy portions **1206** and the conductive material **1212**. The conductive material **1212** may cover the annealed glass paste layer **1206** while touching or not touching the silicon wafer **1204**.

Referring now to FIGS. **33**A-**33**D, alternate integrated circuit packages are show. In FIG. **33**A, an alternate integrated circuit package **1240** includes the annealed glass paste layer **1206** and the conductive material layer **1212**, which are located adjacent to circuit components **1242** of the silicon wafer **1204**. In FIG. **33**B, an alternate integrated circuit package **1250** includes the annealed glass paste layer **1206** and conductive material layer **1212**, which are located adjacent to an oscillator **1252** of the silicon wafer **1204**.

In FIG. **33**C, an alternate integrated circuit package **1260** includes the annealed glass paste layer **1206** and conductive material layer **1212**, which are located adjacent to an inductor **1262** of the silicon wafer **1204**. The inductor **1262** may be an on-chip inductor such as a spiral inductor. In FIG. **33**D, an alternate integrated circuit package **1270** includes the annealed glass paste layer **1206** and conductive material layer **1212**, which are located adjacent to oscillator circuit **1272** with an inductor **1274**.

The annealed glass paste layer also tends to reduce the change in stress over time that can occur. The annealed glass paste layer isolates all or part of the silicon wafer from variations in the dielectric properties such as dielectric loss of the molding material. This can be particularly advantageous when attempting to calibrate using temperature as described above.

Referring now to FIGS. **34**A-**34**D, alternate integrated circuit packages are shown that include annealed glass paste and/or epoxy portions and a glass or silicon layer that create an air gap above portions of a silicon wafer. In FIGS. **34**A-**34**B, integrated circuit packages **1300** and **1330** include a silicon wafer **1304**. Annealed glass paste portions **1306** are formed on the silicon wafer **1304** in a spaced apart relationship. The AGP portions **1306** may be formed as described above. A molding material **1308** may be used. Post-processing of the AGP portions **1306** may be performed such as polishing or other steps to provide a planar outer surface.

A glass or silicon layer **1310** is supported above the silicon wafer **1304** by the AGP portions **1306**. Epoxy or other adhesive binding material may be used to attach the glass or silicon layer **1310** to the AGP portions **1306**. AGP portions **1306** and the glass or silicon layer **1310** form an air gap **1324** above an oscillator **1320** in FIG. **34**A and/or any other circuit **1322** in

FIG. **34**B. The air gap **1324** provides the material (air) having the lowest possible dielectric loss. In contrast, when crystal oscillators are used, the air is needed to allow the crystal to resonate—in other words, the air is used to allow mechanical oscillation.

In FIGS. **34**C-**34**D, integrated circuit packages **1340** and **1360** include a silicon wafer **1304**. Epoxy portions **1342** are formed on the silicon wafer **1304** in a spaced apart relationship. The epoxy portions **1342** may be formed as described above. Post-processing of the epoxy portions **1306** may be performed such as polishing or other steps to provide a planar outer surface. A glass or silicon layer **1310** is supported above the silicon wafer **1304** by the epoxy portions **1342**. Epoxy or other adhesive binding material may be used to attach the glass or silicon layer **1310** to the epoxy portions **1342**. The portions **1306** and the layer **1310** form an air gap **1324** above an oscillator **1320** in FIG. **34**C and/or any other circuit **1322** in FIG. **34**D.

Referring now to FIGS. **35**A-**35**B, alternate integrated circuit packages are shown that include a glass or silicon portion that creates an air gap. In FIG. **35**A, an integrated circuit package the **1380** includes a "C"-shaped glass or silicon portion **1382** that defines an air gap **1384**. The "C"-shaped glass or silicon portion **1382** may include multiple sections that are joined together. The air gap **1384** is located above an oscillator **1320**. In FIG. **35**B, an integrated circuit package **1390** includes a "C"-shaped glass or silicon layer **1382** that defines an air gap **1384**. The air gap **1384** is located above a circuit **1322**.

Referring now to FIGS. **36**A-**36**C, methods for making integrated circuit packages described above are shown. An integrated circuit structure **1400** includes a silicon wafer **1404**, a plurality of spaced AGP and/or epoxy portions **1410**A and **1410**B (collectively portions **1410**), and a glass or silicon layer **1408**. The integrated circuit structure **1400** is cut into sections along dotted cutlines **1414** to create multiple integrated circuits, which can be packaged in a molding material (not shown) as described above.

In FIG. **36**B, the silicon wafer **1404** may include one or more bond pads **1420**. Cutting of the layer **1408** at **1414-1** and **1414-2** may be offset from the cutting of the silicon wafer at **1414-3** to provide clearance for attaching bondwires (not shown) to the bond pads **1420**. In FIG. **36**C, one of the integrated circuits **1450** is shown after being separated from the integrated circuit structure **1400**.

Referring now to FIGS. **37**A-**37**B, an integrated circuit package **1450** includes a silicon wafer with spaced annealed glass paste and/or epoxy portions **1410** that have been coated with a layer of conductive material **1456'** are shown. In FIG. **37**A, the portions **1410** are dipped into a container **1454** that contains the conductive material **1456**. The silicon wafer **1408** may be diced along one or more cutlines **1462** and may include bond pads **1460** as shown.

Referring now to FIG. **38**, steps of a method **1500** for fabricating the integrated circuit packaging of FIGS. **32**A-**33**D are shown. Control begins in step **1502**. In step **1504**, a glass paste layer **1206** is applied to one or more surfaces of the silicon wafer **1204** and/or select areas of the silicon wafer **1204**. In step **1506**, the glass paste layer **1204** is annealed by placing the silicon wafer **1204** and the glass paste layer **1204** in an oven. The temperature of the oven may be set to a temperature that is sufficient to cure the glass paste layer **1204**. For example, a temperature of around 400° C. for a predetermined period is sufficient to anneal the glass frit paste while not damaging the silicon wafer **1204**. In step **1508**, the conductive material layer **1212** is applied to the annealed glass paste layer **1204**. In step **1510**, all or part of the silicon wafer **1204** is encased in a molding material **1208** such as plastic, other materials described herein, and/or other suitable molding materials. In step **1520**, control ends.

In each of the foregoing embodiments, the silicon wafer may be replaced by other wafers or other substrates and the annealed glass paste can be replaced by epoxy.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:

1. A system for configuring a semiconductor device to generate an output signal, the system comprising:

a temperature sensor configured to sense a plurality of operating temperatures of the semiconductor device, the plurality of operating temperatures including at least (i) a first operating temperature, and (ii) a second operating temperature;

a controller configured to determine a plurality of operating frequencies of the output signal at respective operating temperatures of the plurality of operating temperatures, the plurality of operating frequencies including (i) a first operating frequency of the output signal when the semiconductor device is at the first operating temperature, and (ii) a second operating frequency of the output signal when the semiconductor device is at the second operating temperature; and

memory configured to store calibration information, wherein the calibration information associates each of the plurality of operating temperatures of the semiconductor device with respective operating frequencies of the plurality of operating frequencies.

2. The system of claim **1**, further comprising a heater configured to heat the semiconductor device to increase the first operating temperature of the semiconductor device to the second operating temperature of the semiconductor device.

3. The system of claim **1**, wherein the calibration information further associates, for each of the plurality of operating frequencies, a plurality of temperature indicators with respective correction factors.

4. The system of claim **3**, wherein the controller is further configured to (i) select an operating frequency from the plurality of operating frequencies, (ii) generate a control input to control the output signal according to the selected operating frequency, (iii) determine, for the selected operating frequency, a first temperature indicator of the plurality of temperature indicators, (iv) select, based on the first temperature indicator, a first correction factor from the respective correction factors, and (v) adjust the control input based on the first correction factor to maintain the selected operating frequency.

5. The system of claim **4**, wherein the respective correction factors correspond to ratios to be applied to the control input according to the plurality of temperature indicators.

6. The system of claim **3**, wherein the calibration information includes a table associating the plurality of temperature indicators to the respective correction factors.

7. The system of claim **3**, wherein the plurality of temperature indicators correspond to respective sensed temperatures of the semiconductor device.

8. The system of claim **3**, wherein the plurality of temperature indicators correspond to respective changes in temperature from a calibration temperature associated with the semiconductor device to a sensed temperature of the semiconductor device.

9. The system of claim 8, wherein the calibration temperature corresponds to the first operating temperature and the sensed temperature corresponds to the second operating temperature.

10. The system of claim 8, wherein the calibration temperature corresponds to a lowest operating temperature of the semiconductor device.

11. A method for configuring a semiconductor device to generate an output signal, the method comprising:

sensing a plurality of operating temperatures of the semiconductor device, the plurality of operating temperatures including at least (i) a first operating temperature, and (ii) a second operating temperature;

determining a plurality of operating frequencies of the output signal at respective operating temperatures of the plurality of operating temperatures, the plurality of operating frequencies including (i) a first operating frequency of the output signal when the semiconductor device is at the first operating temperature, and (ii) a second operating frequency of the output signal when the semiconductor device is at the second operating temperature; and

storing, in a memory, calibration information, wherein the calibration information associates each of the plurality of operating temperatures of the semiconductor device with respective operating frequencies of the plurality of operating frequencies.

12. The method of claim 11, further comprising heating the semiconductor device to increase the first operating temperature of the semiconductor device to the second operating temperature of the semiconductor device.

13. The method of claim 11, wherein the calibration information further associates, for each of the plurality of operating frequencies, a plurality of temperature indicators with respective correction factors.

14. The method of claim 13, further comprising (i) selecting an operating frequency from the plurality of operating frequencies, (ii) generating a control input to control the output signal according to the selected operating frequency, (iii) determining, for the selected operating frequency, a first temperature indicator of the plurality of temperature indicators, (iv) selecting, based on the first temperature indicator, a first correction factor from the respective correction factors, and (v) adjusting the control input based on the first correction factor to maintain the selected operating frequency.

15. The method of claim 14, wherein the respective correction factors correspond to ratios to be applied to the control input according to the plurality of temperature indicators.

16. The method of claim 13, wherein the calibration information includes a table associating the plurality of temperature indicators to the respective correction factors.

17. The method of claim 13, wherein the plurality of temperature indicators correspond to respective sensed temperatures of the semiconductor device.

18. The method of claim 13, wherein the plurality of temperature indicators correspond to respective changes in temperature from a calibration temperature associated with the semiconductor device to a sensed temperature of the semiconductor device.

19. The method of claim 18, wherein the calibration temperature corresponds to the first operating temperature and the sensed temperature corresponds to the second operating temperature.

20. The method of claim 18, wherein the calibration temperature corresponds to a lowest operating temperature of the semiconductor device.

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